KU LEUVEN

Challenges and Radiation Performances of Advanced and Emerging CMOS Technologies

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Fellow IEEE, Fellow ECS

Outline

Basic Radiation Effects & Scaling Trends

- **Basic Radiation Effects**
- **Low Temperature Operation & Radiation**
- **Trends in Microelectronics**
- **Important Process Modules Impacting Radiation Hardness**

Impact Device Technology on Radiation Performance

- **Bulk and SOI FinFETs**
- **Ultra Thin Body and BOX (UTBOX)**
- **TunnelFETS (TFETs)**
- **Resistive Memories (ReRAMs)**
- **SiGe Channel Devices**
- **Ge-based Devices**

Conclusions

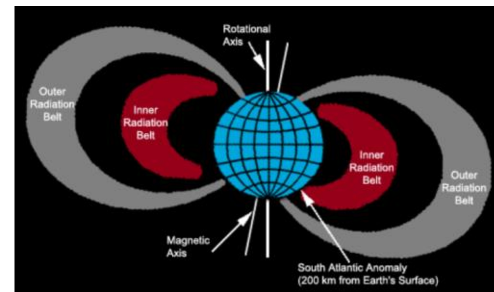
Justifications

High Flux environment

- Large Hadron Collider (CERN, Berkeley)
- Fusion Reactor in France
- Nuclear facilities (maintenance, robot handling, dismantling...)

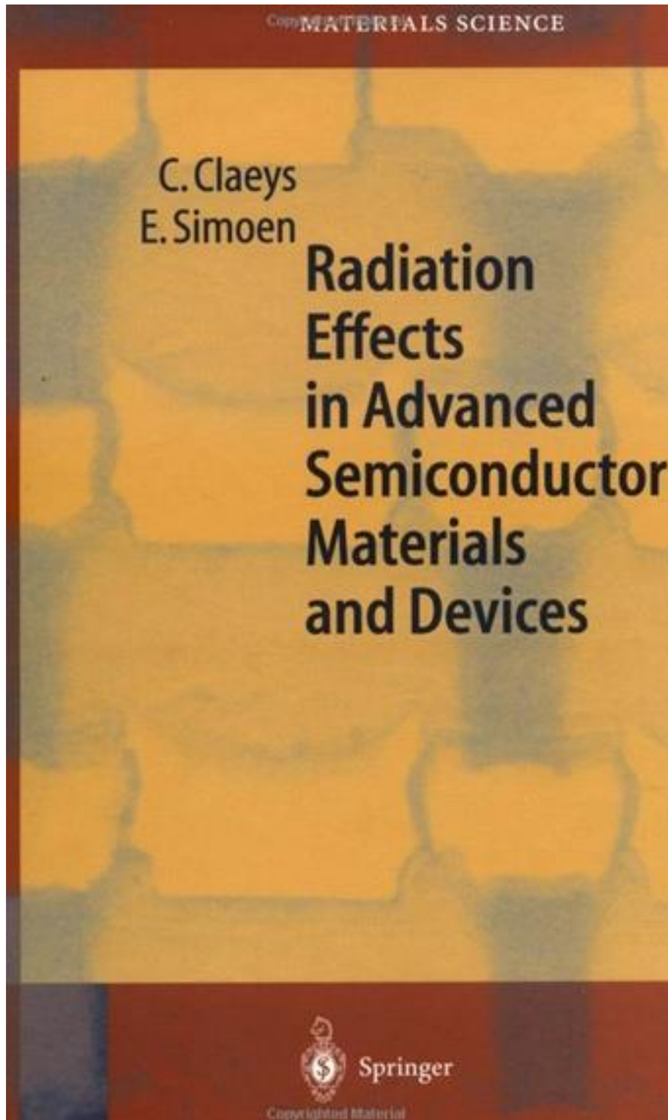
Space Application

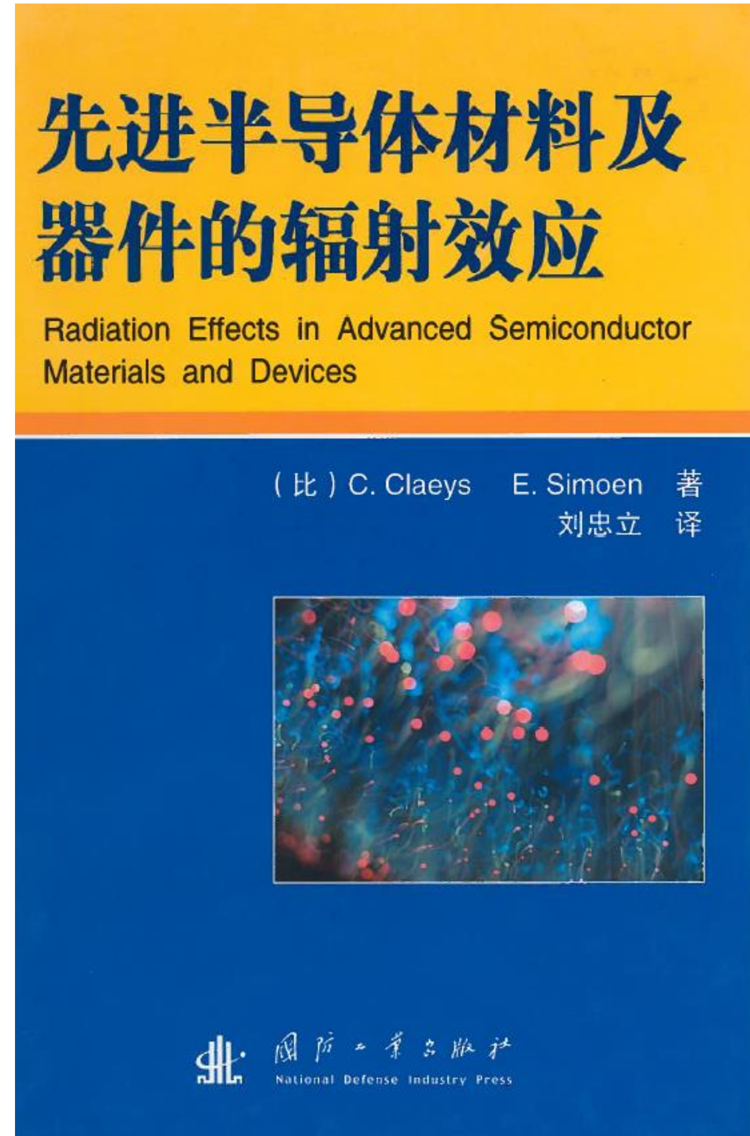
- Radiation particle f(orbit)
- South Atlantic Anomaly (SAA) high energetic particles



Radiation in Microelectronics (Packages)

Further Reading





Basic Concepts

Ionizing Damage: creation of electron-hole pairs across the band gap

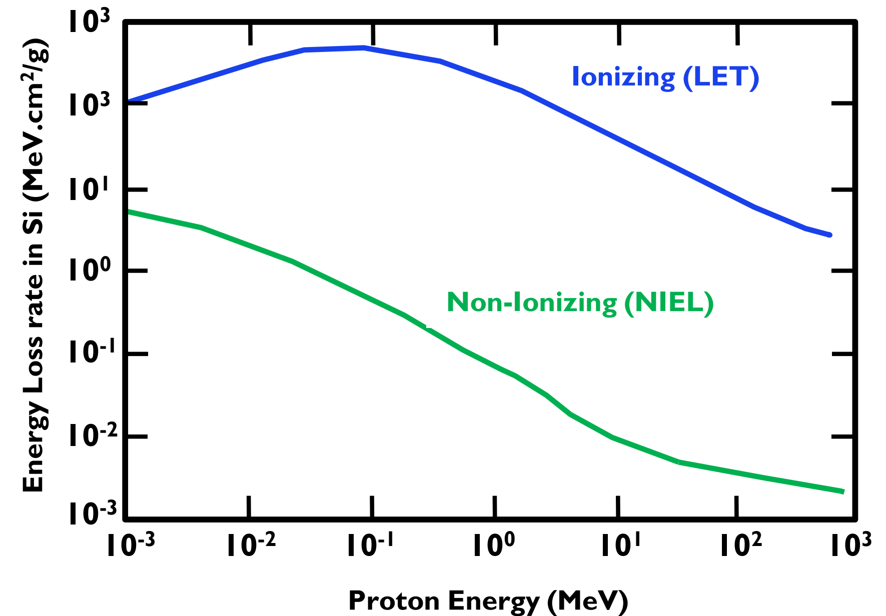
- **Scales with the Linear Energy Transfer (LET) function.**
- **Important for dielectrics in MOS: gate and field oxide.**
- **Irradiation: Generation electron-hole pairs**
  - **Linear Energy Transfer (LET) function (in MeV cm^2/g)**
  - **1 Gray=1 J/kg=100 rad**

Displacement Damage: creation of vacancy-interstitial (V-I) pairs by displacement of a lattice atom

- **Scales with the Non-Ionising Energy Loss (NIEL) parameter.**
- **Not so relevant for MOS devices (bipolar devices; diode;…).**

Ionization and Displacement Damage =f(particle, energy)

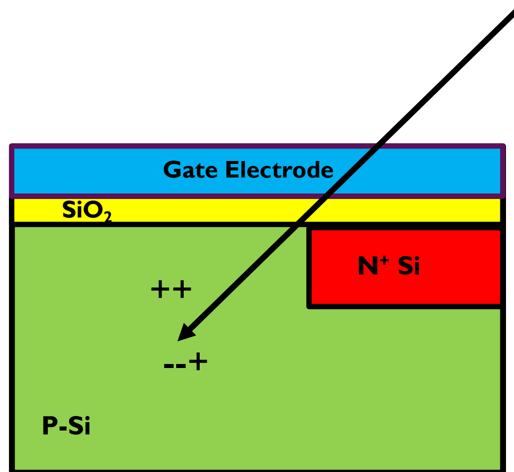
The energy loss rate through ionization and excitation of the Si lattice (LET) and through atomic displacements (NIEL) versus proton energy.



Proton irradiation

For protons only a fraction of 1% of the energy loss goes into displacement processes

Ionizing Damage in MOS



Gate: carries away the charge

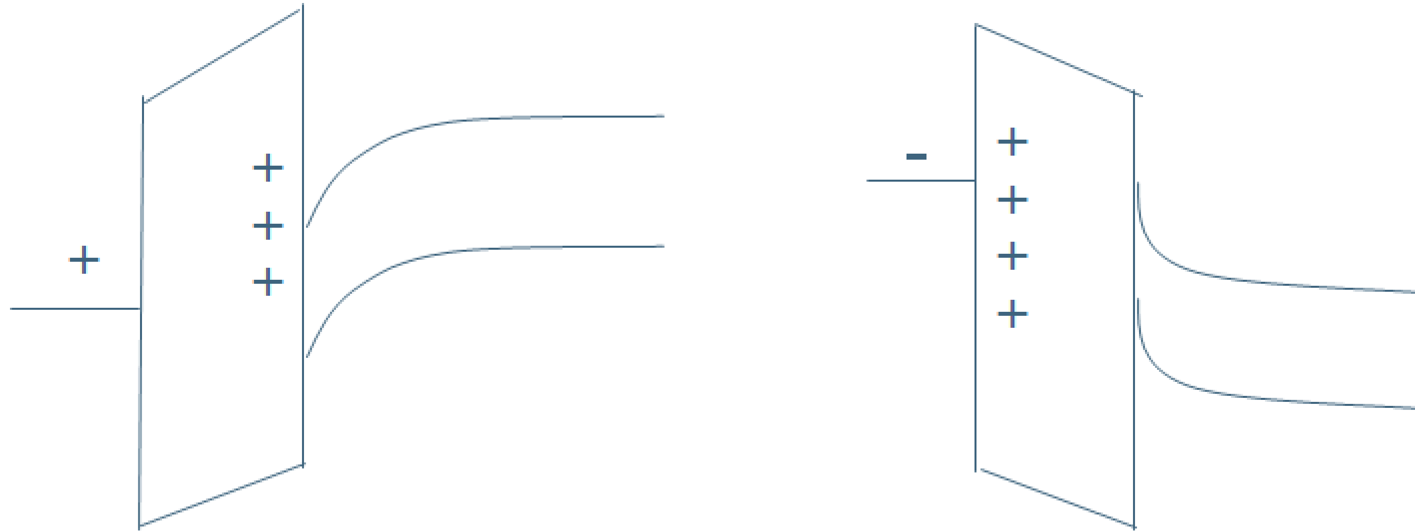
Silicon: electron-hole pairs can recombine in the neutral bulk

In case of a p-n junction, the electric field separates electrons and holes. This leads to a transient charging phenomenon

➔Single Event Upsets (SEU)

Permanent ionizing damage only in the dielectric layers: gate oxide, isolation or field oxide and buried oxide (SOI)

Ionizing Damage in MOS

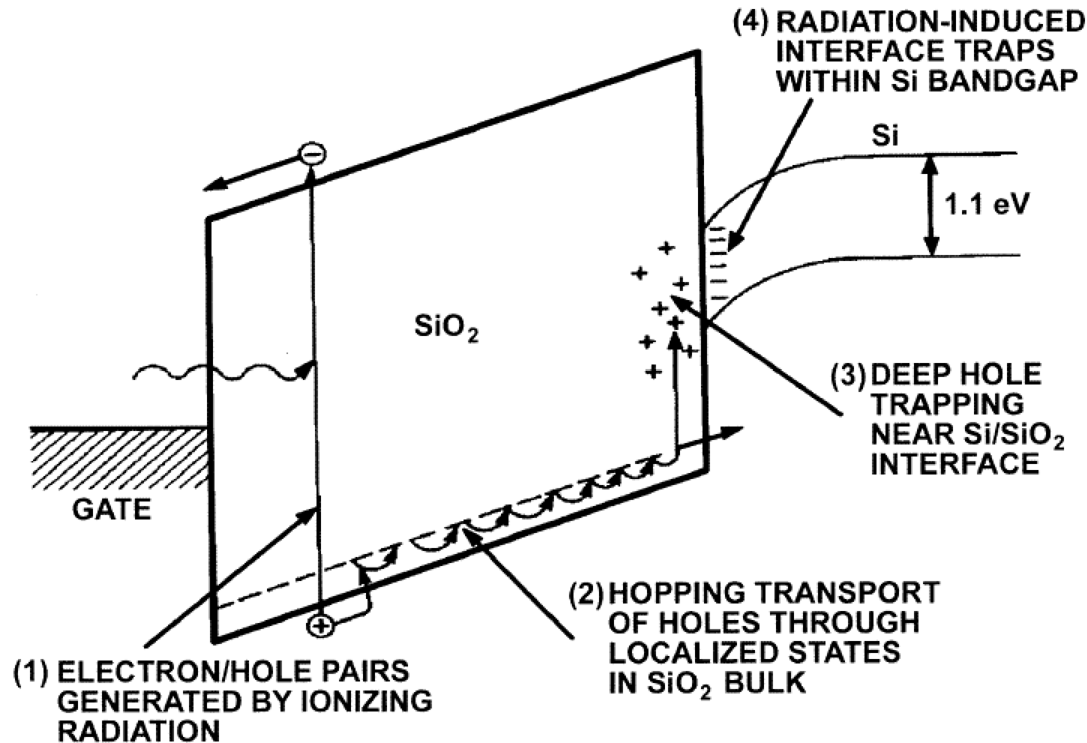


Trapped hole charge has a stronger impact for positive gate bias (nMOS)

➔ degradation of nMOS stronger, because holes are drifting towards the Si-SO_2 interface

➔ importance of biased radiation testing

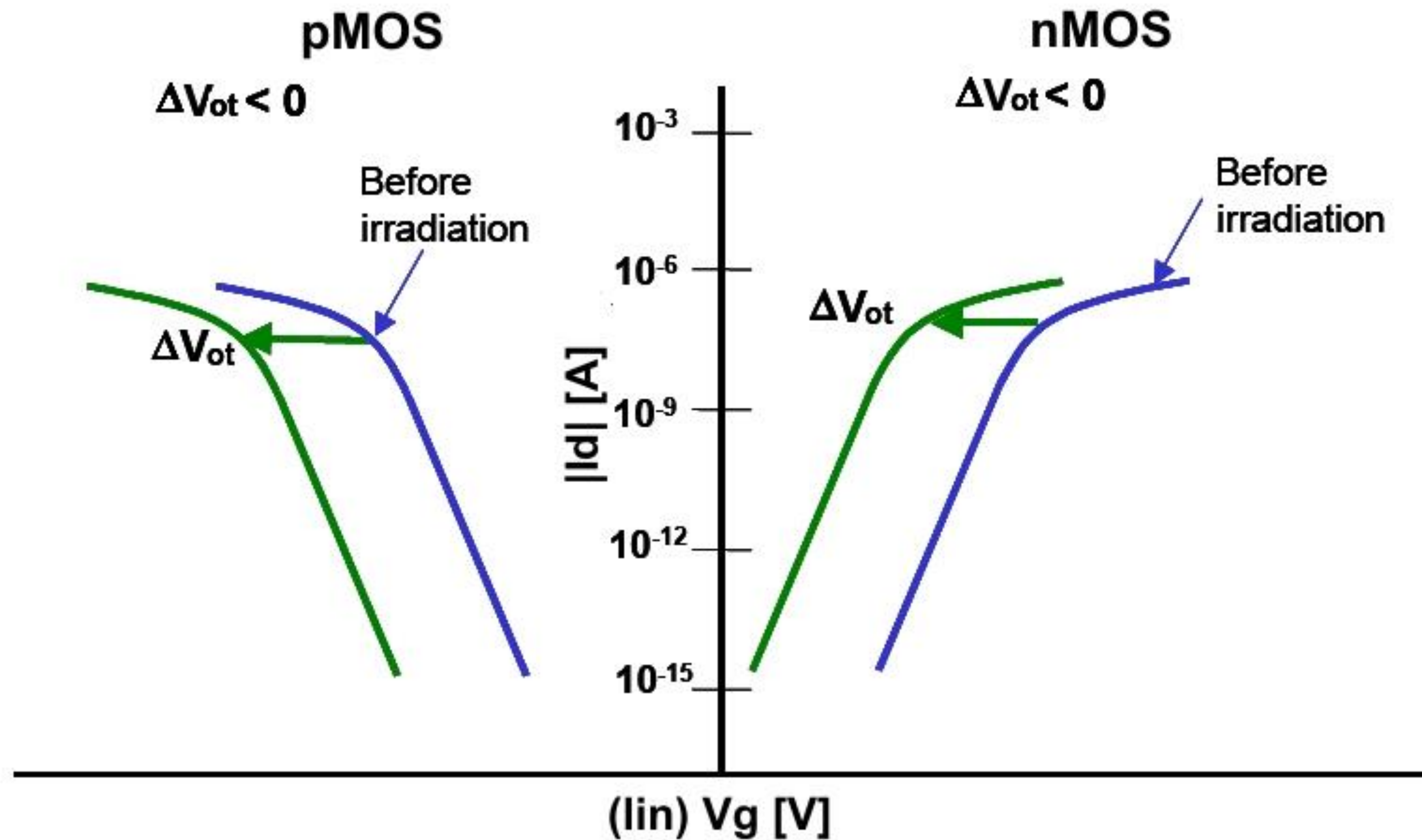
Ionizing Damage in MOS



N_{ot} & N_{it}

T. R. Oldham and F. B. McLean, IEEE Trans. Nucl. Sci., 50, 483 (2003)

Effects of Oxide Traps



Oxide traps are always positively charged

Effects of Interface Traps

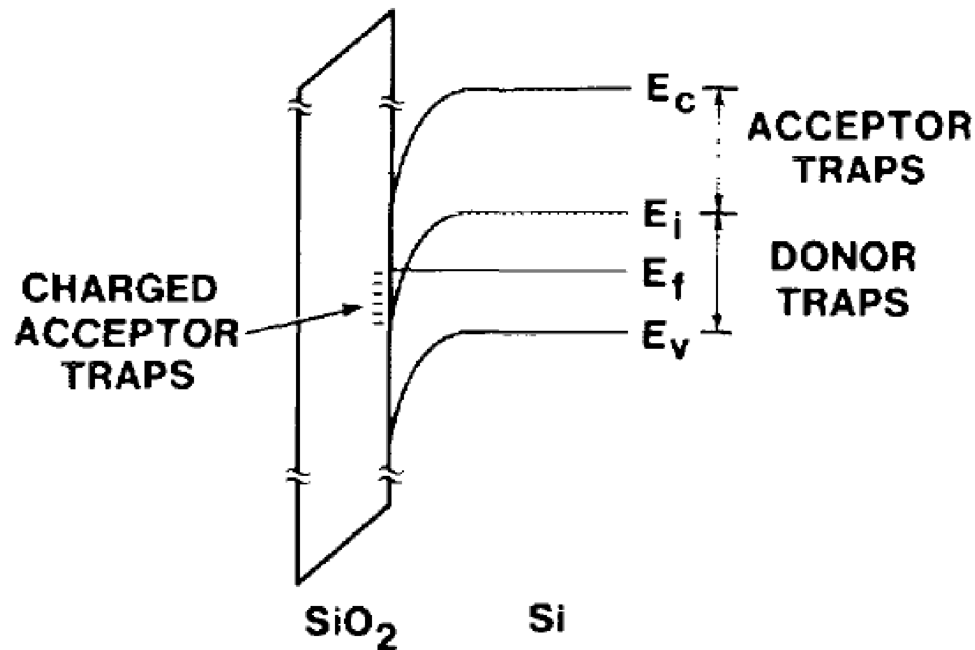
- **Related to dangling bond defects**

- **Unpaired electron on a Si atom that is back-bounded to 3 other Si atoms at the Si/SiO_2-interface**

- **Studied type is amphoteric: can be negatively or positively charged**

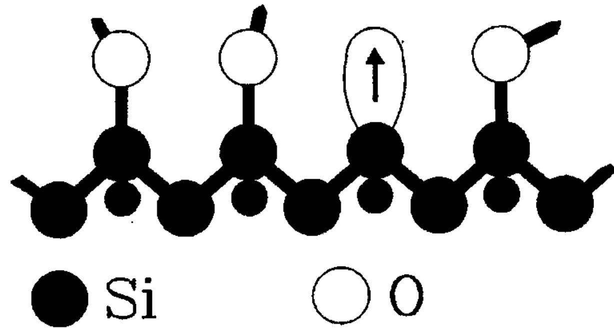
- **Interface traps can have a significant effect on the potential, mobility and recombination rates at the semiconductor surface**

Effects of Interface Traps

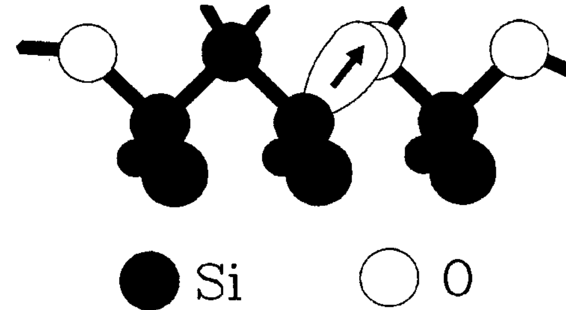


N_{it} – negative in nMOS and positive in pMOS due to the band bending

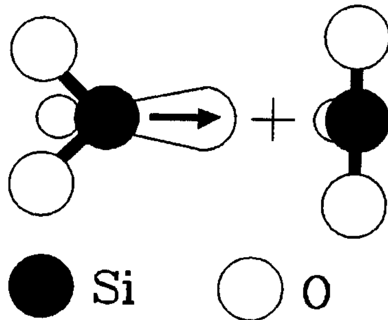
Effects of Interface Traps



(100) Si-SiO_2



(111) Si-SiO_2

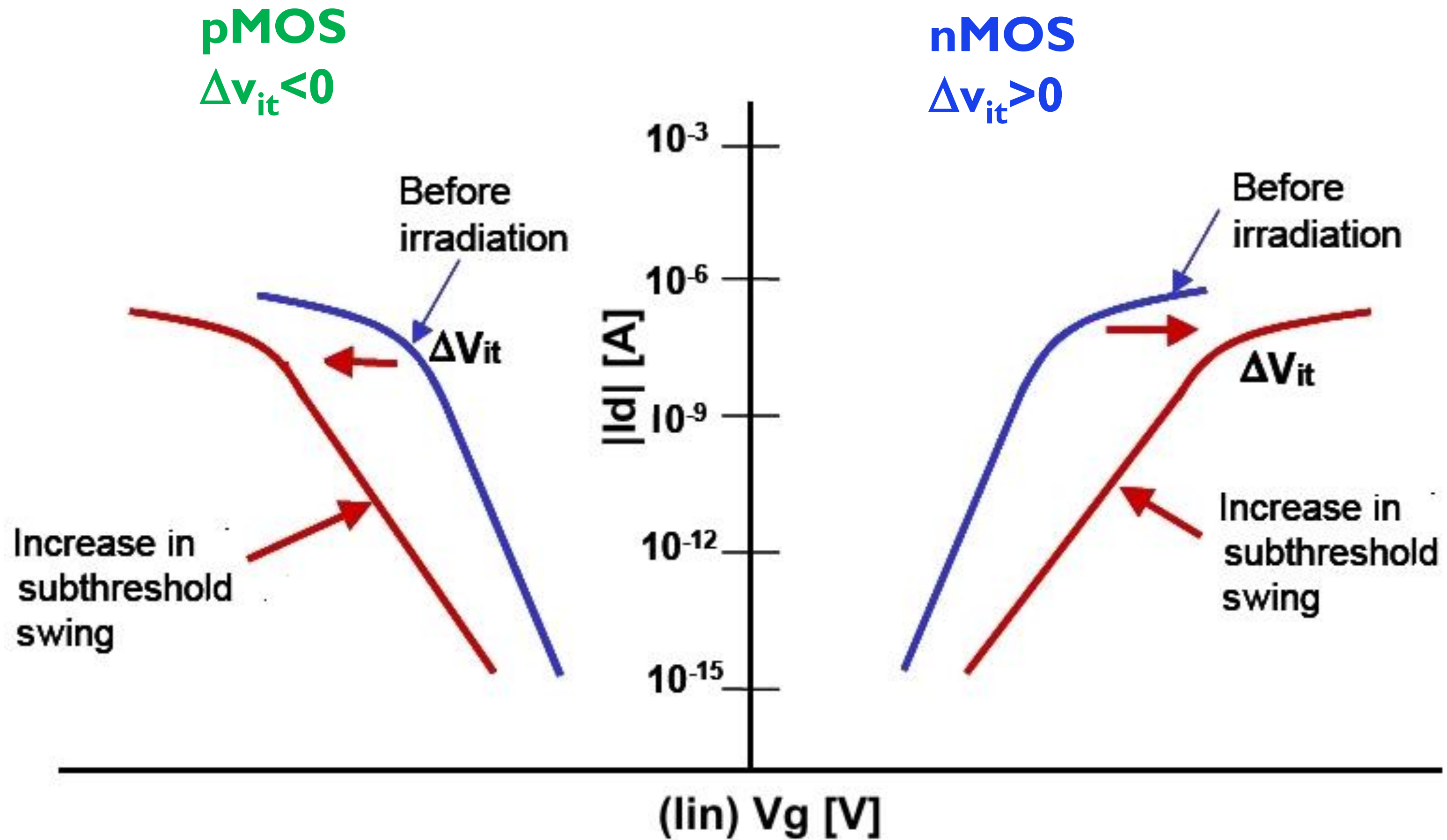


These radiation-induced defects have been identified by ESR.

Role of hydrogen !!!

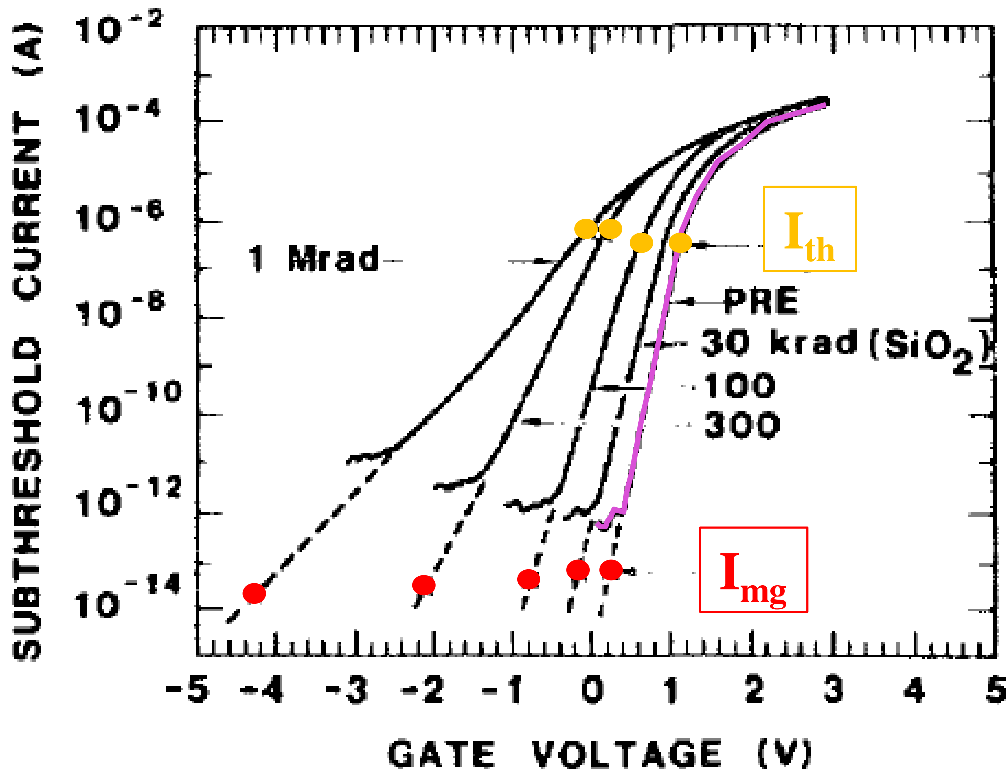
PM Lenahan and JF Conley J., J. Vac.Sci. Techol. B 16, pp. 2134-2153 (1998).

Effects of Interface Traps



Interface traps are positively charged in pMOS and negatively charged in nMOS

Separation Effects of Oxide and Interface Traps



I_{th} – current at threshold
I_{mg} = midgap current when

$$\phi_b = (kT/q) \ln (N_A/n_i)$$

Stretch-out voltage

$$V_{so} = V_{th} - V_{mg}$$

$$\Delta V_{N_{it}} = (V_{so})_2 - (V_{so})_1$$

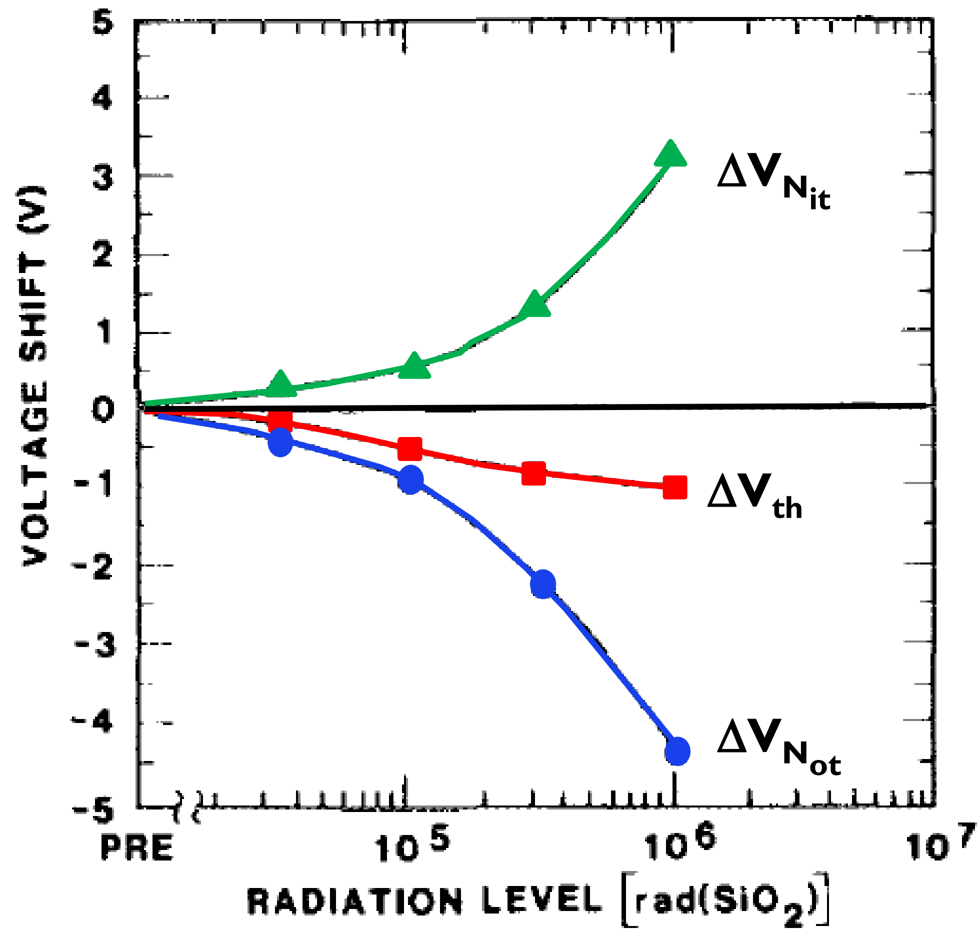
$$\Delta N_{it} = \Delta V_{N_{it}} C_{ox}/q$$

$$\Delta V_{N_{ot}} = (V_{mg})_2 - (V_{mg})_1.$$

$$\Delta N_{ot} = C_{ox} \Delta V_{N_{ot}}/q.$$

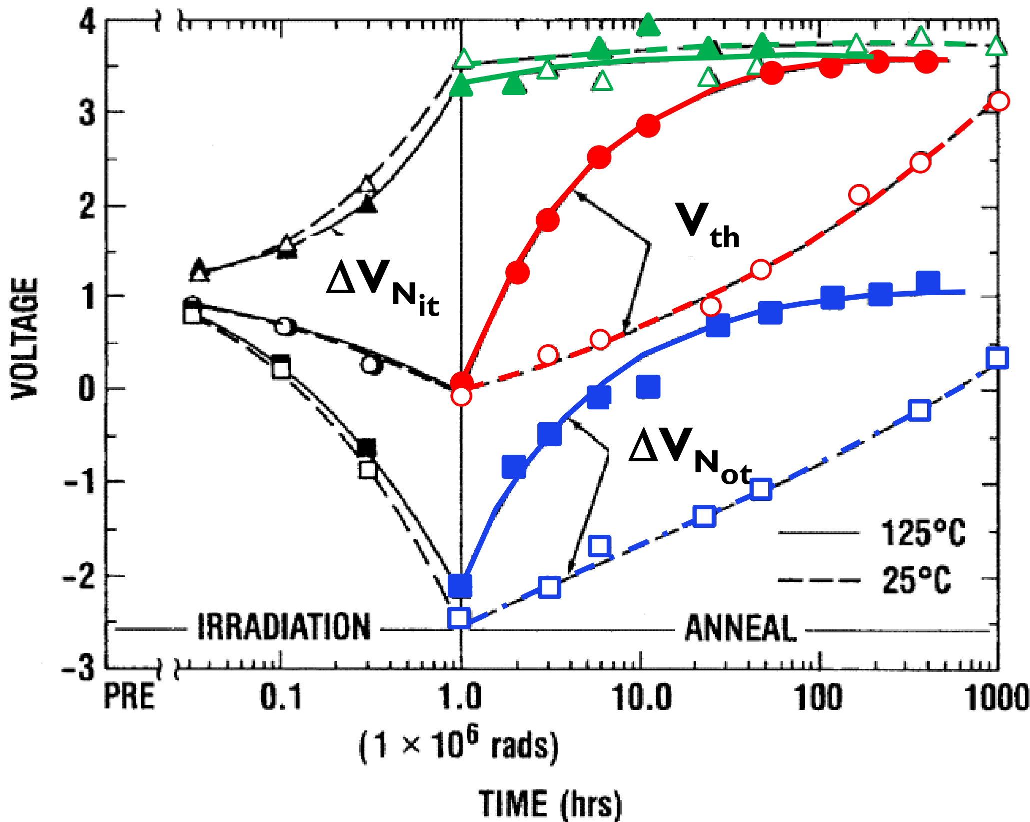
P.J. McWhorter and P.S. Winokur, APL, 48, 133 (1986)

Separation Effects of Oxide and Interface Traps



P.J. McWhorter and P.S. Winokur, APL, 48, 133 (1986)

Annealing – Rebound Effect



- Device will fail after 1 Mrad due to the trapped oxide charge ΔV_{OT}
- After annealing the ΔV_{OT} reduces and the device may operate again as holes anneal out
- Further annealing may cause again the device to fail due to the interface charge, which doesn't anneal much during the anneal step (<100˚C)
- For high anneal temperatures also the interface traps anneal out

Rebound effect

Note: For TID effects in CMOS devices the dose rate has no impact

T. R. Oldham and F. B. McLean, IEEE Trans. Nucl. Sci., 50, 483 (2003)

Device Scaling

$$\Delta V_t \sim t_{ox}^2$$

Good TID resistance of the thin Gate oxide

Radiation effects will be caused by parasitic conduction related to

Shallow Trench Isolation oxide: Bulk

Buried oxide for SOI devices

Occurrence of other radiation related phenomena

Transient Mechanisms

- **Single Event Upset - SEU**

  Collected charge may cause 0<->1

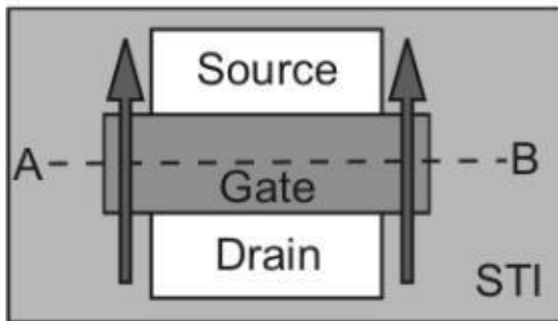
  Scaling is generally worsens SEU: The smaller the memory node the smaller the charge needed for to upset

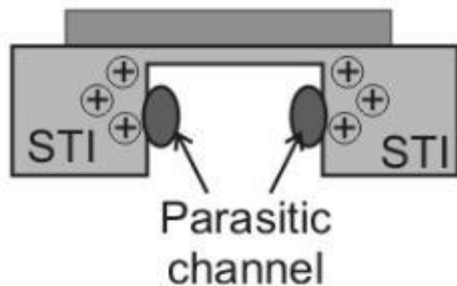
- **Single Event Latch Up - SEL**

  Firing of the parasitic thyristor in CMOS is destructive

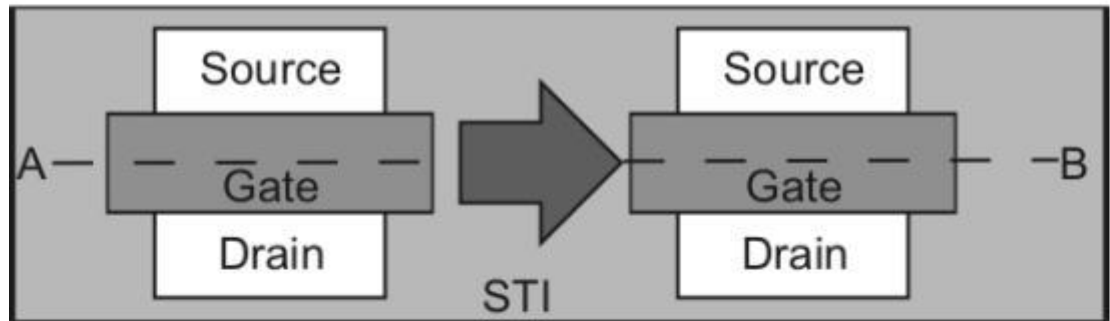
Leakage in CMOS Devices

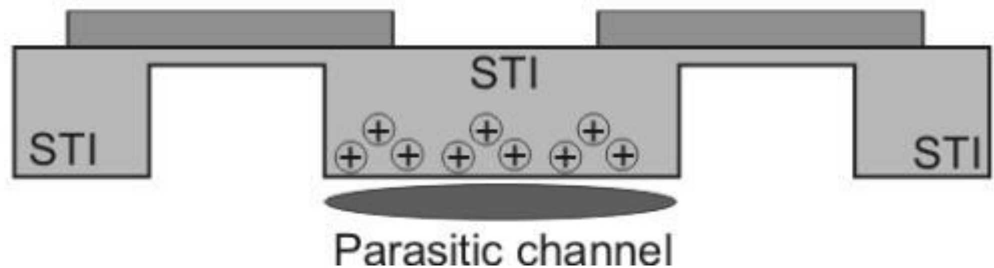
Edge leakage





Inter-leakage





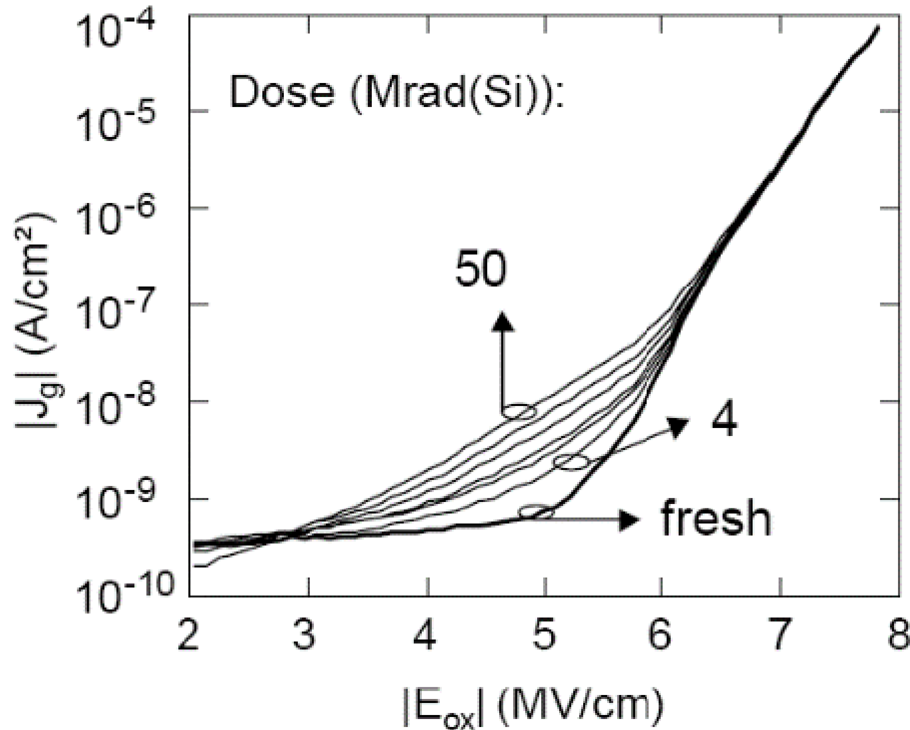
Impact High Energy Ions on gate Oxide

Radiation-Induced Leakage Current (RILC)

Radiation-Induced Soft Breakdown (RSB)

Increase of off-state power consumption
but no real concern

Radiation Induced Leakage Current

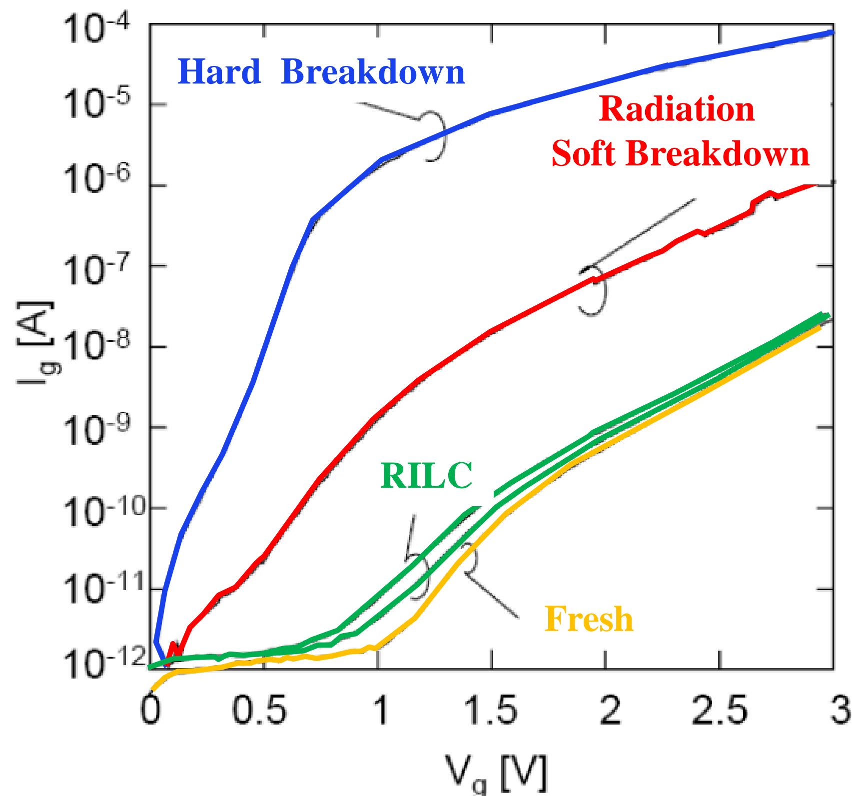


Negative J_g-E_{ox}, curves measured before (fresh) and after irradiation for various doses ranging from 4 to 50 Mrad(Si). 6 nm oxide.

- **Increase of the low field current between 3and 6 MV/cm**
- **Can be attributed to RILC which is similar to SILC – trapped holes**
- **Important to study the involved kinetics**
  - **RILC has no saturation of current versus dose**
  - **SILC has a saturation of current versus injected charge.**

M. Ceschia A. Paccagnella, A. Cester, A.Scarpa and G. Ghidini, IEEE Trans. Nucl. Sci., 45, pp. 2375-2382 (1998)

Ion Induced Degradation of Gate Dielectrics

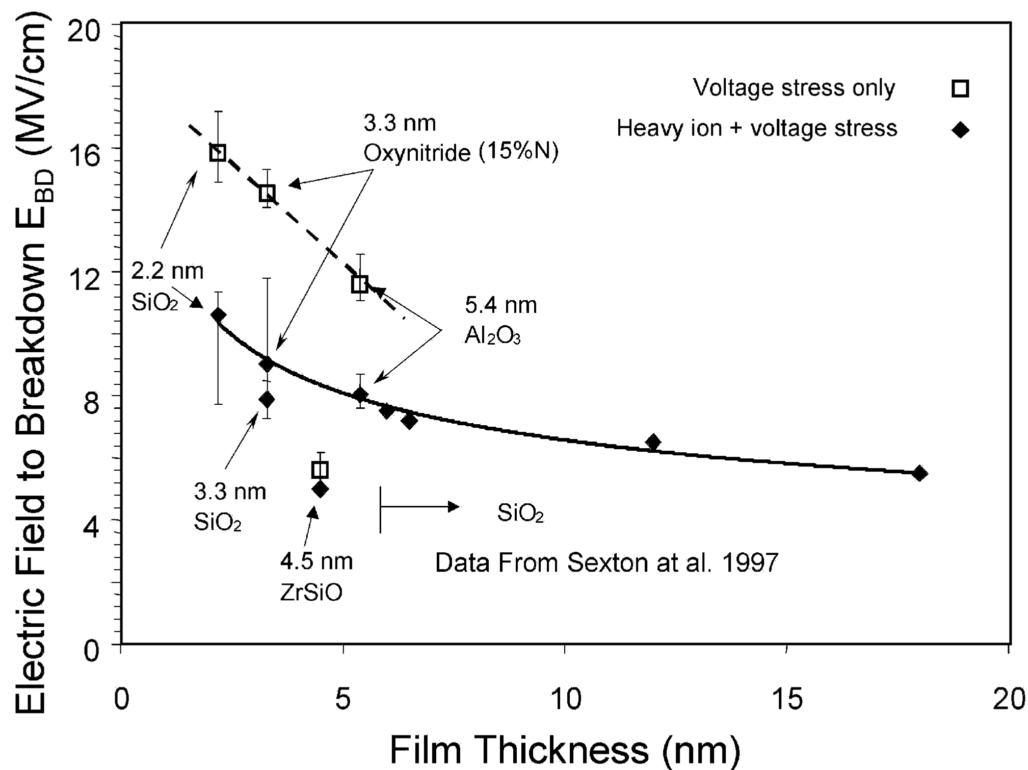


Gate current versus gate voltage (Ig–Vg) measured before and after irradiation on a 3-nm oxide. The two curves referring to RILC have been measured after irradiation with 5.8×10^{10} and 1.5×10^{11} Si ion/cm . The RSB has been obtained after irradiation with 10^{7} I ions/cm .

- Radiation-induced soft breakdown (RSB) is observed in 3-and 4-nm oxides only after irradiation with high linear energy transfer (LET)
- Only RSB and SEGR (single event gate rupture) appear as the main factors limiting the device lifetime, while RILC can be important for applications as EPROM-like memories

A. Cester, L. Bandiera, M. Ceschia, G. Ghidini and A. Paccagnella, IEEE Trans. Nucl. Sci., 48, pp. 2093-2100 (2001)

Single Event Gate Rupture

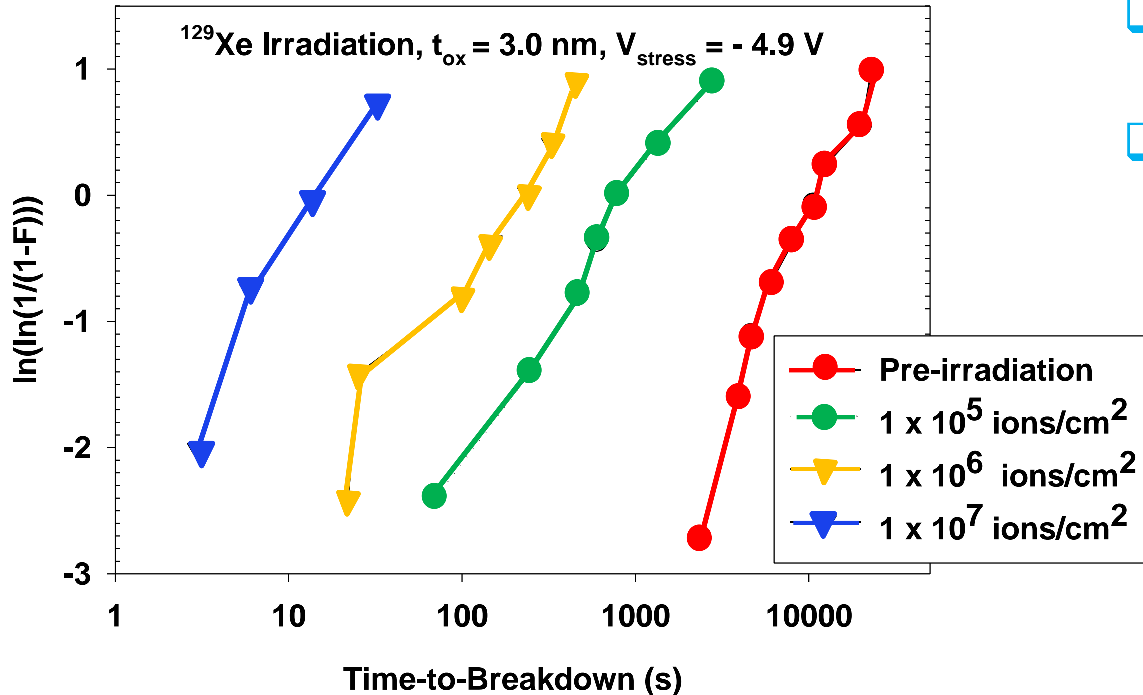


SEGR

- Operating voltage lower than critical value
- Critical LET threshold

L.W. Massengill, B.K. Choi, D.M. Fleetwood, R.D. Schrimpf, M.R. Shaneyfelt, T.L. Meisenheimer, P.E. Dodd, J.R. Schwank, Y.M. Lee, R.S. Johnson and G. Lucovsky, IEEE Trans. Nucl. Sci., 48, pp. 1904-1912 (2001)

Latent radiation Damage in Thin Gate Oxide



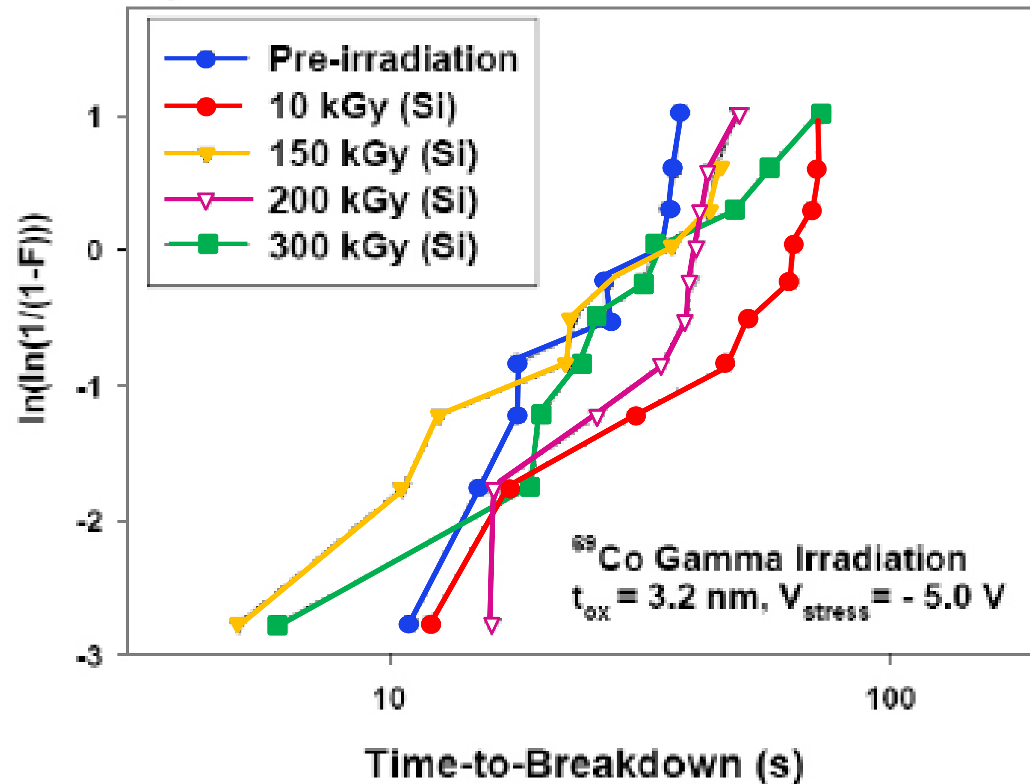
- No parameter shift after irradiation only
- Reduced oxide lifetime after accelerated testing

LET > 30 MeV/cm^2

Weibull lifetime distribution of MOS capacitors subjected to constant voltage stress at V_{stress}=-4.9 V before and after heavy ion irradiation

J.S. Suehle, E.M. Vogel, P. Roitman, J.F. Conley Jr., J.B. Bernstein and C.E. Weintraub, Appl. Phys. Lett., 80, pp. 1282-1284 (2002)

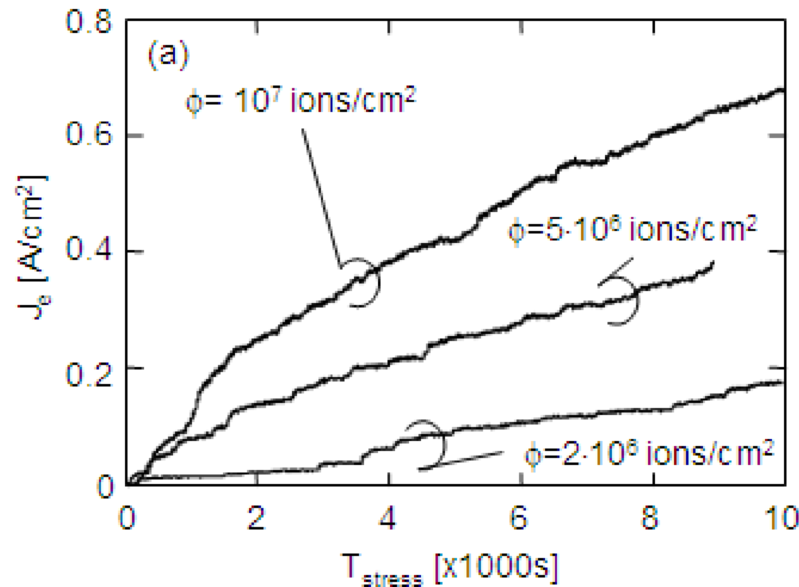
Latent radiation Damage in Thin Gate Oxide



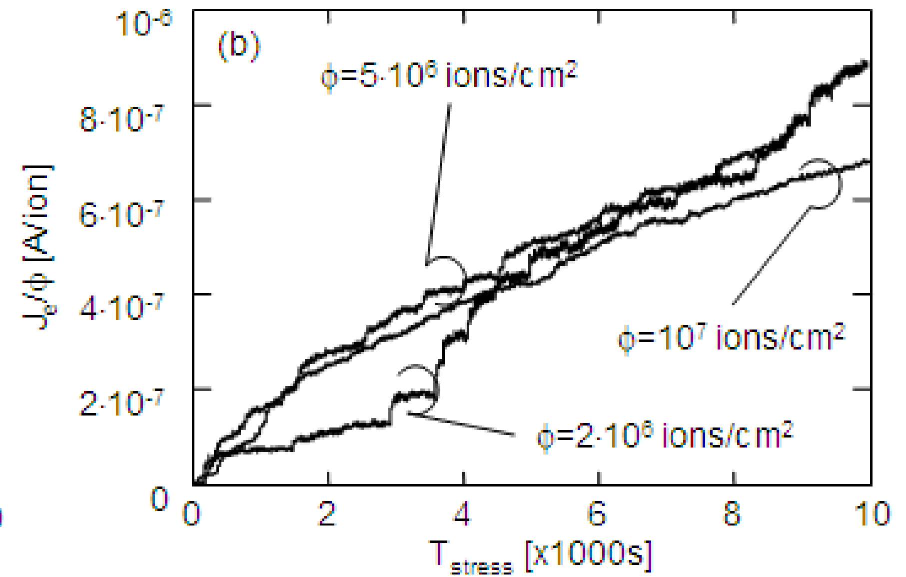
Weibull lifetime distribution of MOS capacitors subjected to constant voltage stress at V_{stress}=-5.0 V before and after ^{60}Co irradiation.

J.S. Suehle, E.M. Vogel, P. Roitman, J.F. Conley Jr., J.B. Bernstein and C.E. Weintraub, Appl. Phys. Lett., 80, pp. 1282-1284 (2002)

Latent Radiation Damage – Ion Fluence



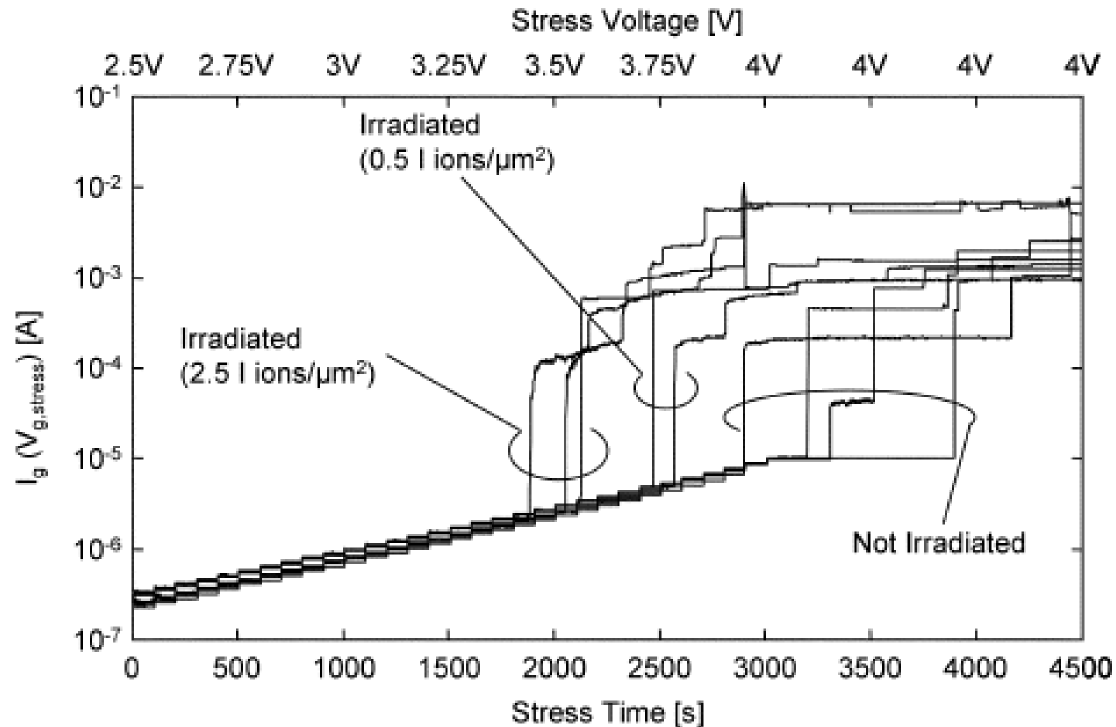
Gate current during CVS at V_{CVS} = 4.2 V on three samples with gate area 10^{-2} cm^2 irradiated with 256-MeV I ions at different fluences



Excess gate current Density (J_e) normalized to the ion fluence (ϕ) measured during CVS at V_{CVS}=4.2 V

A. Cester, S. Cimino, E. Miranda, A. Candelori, G. Ghidini and A. Paccagnella, IEEE Trans. Nucl. Sci., 50, pp. 2167 2175 (2003)

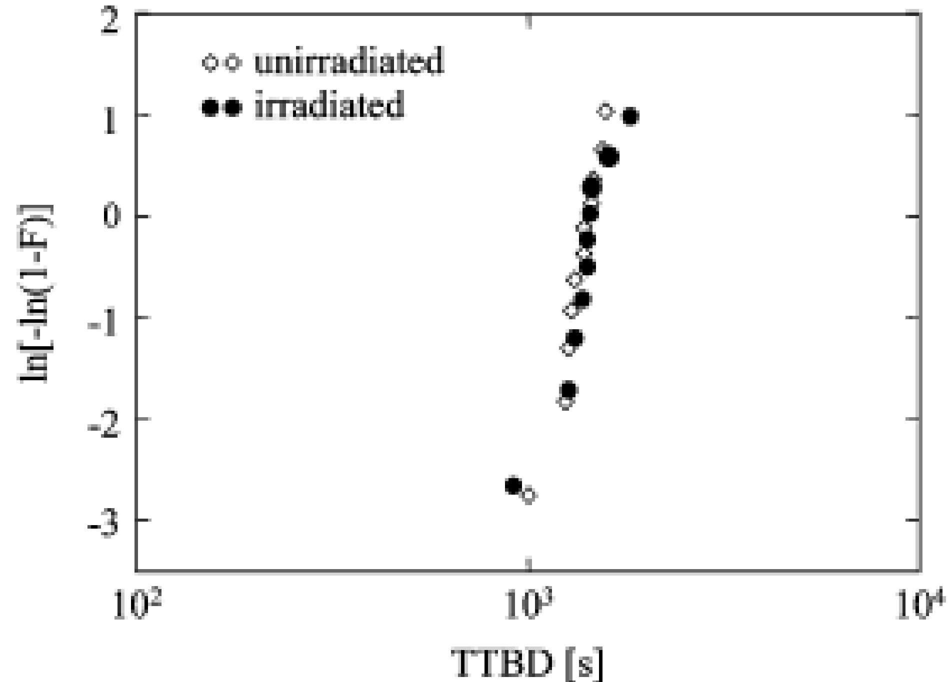
100 nm PD SOI Technology
10-20% change f(ion fluence)
Staircase Voltage Stress



Gate current measured at $V_g = V_{g,stress}$ during FN injection of devices processed in an 0.1 µm PD SOI technology. $V_{g,stress}$ starts from 2.5 V and increases up to 4 V with 50-mV step every 100 s. The stress was performed on fresh and irradiated devices with two different ion fluences (2.5 and 0.5 I ions/mm²).

A. Cester, S. Gerardin, A. Paccagnella, E. Simoen and C. Claeys, IEEE Trans. Nucl. Sci., 52, pp. 2252-2258 (2005)

65nm Technology

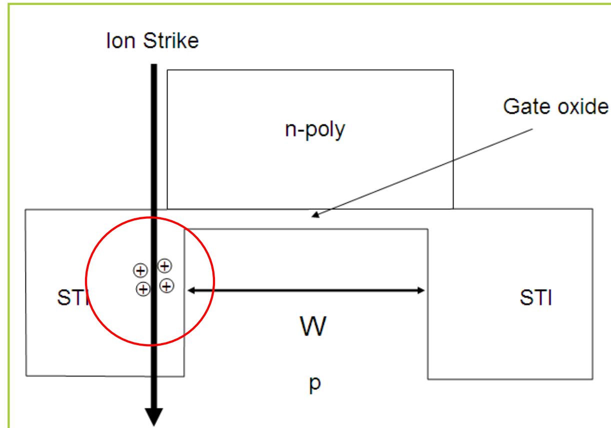


Gate current time to breakdown for irradiated (2.5 I ions/mm^2) and non-irradiated FD SOI MOSFETs (W=L = 10 µm/10 µm) fabricated in a 65 nm technology with different strain levels.
The devices were stressed with a staircase voltage from 2 V to 4 V with 50-mV steps, each lasting 100 s.

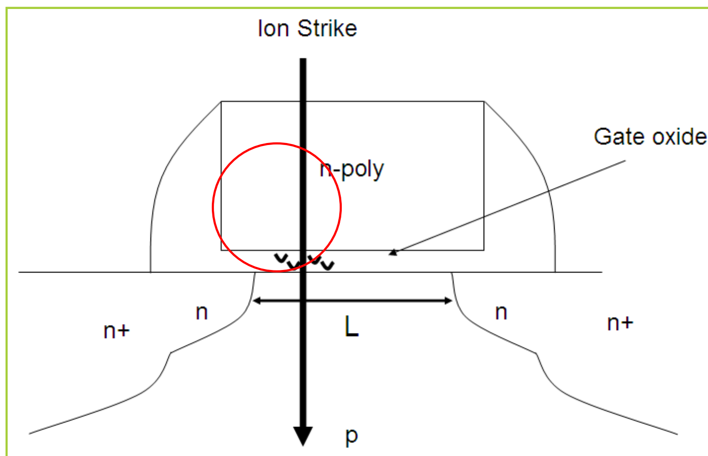
A. Griffoni, S. Gerardin, A. Cester, A. Paccagnella, E. Simoen and C. Claeys, IEEE Trans. Nucl. Sci., 54, pp. 2257-2263 (2007)

Heavy Ion Strikes: Microdose Effects

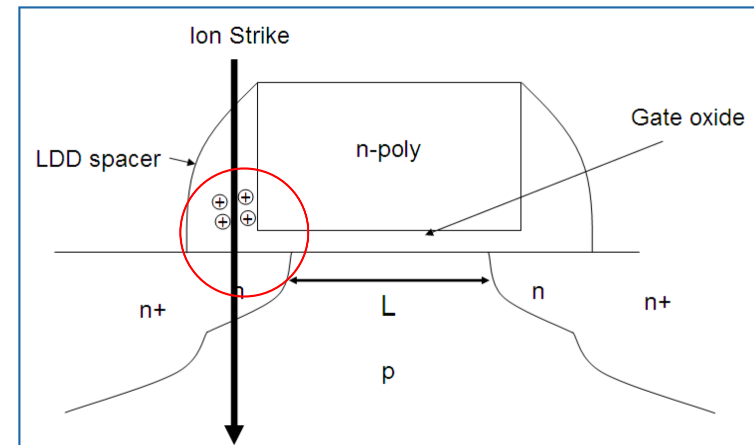
charge build-up in the STI



Defect generation in the oxide



charge build-up in the LDD region

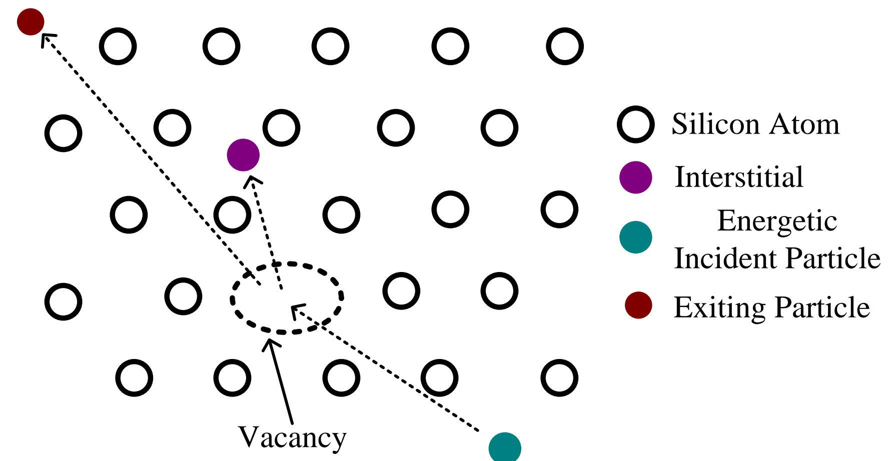


Statistical in nature

S. Gerardin, M. Bagatin, A. Cester, A. Paccagnella and B. Kaczer, IEEE Trans. Nucl. Sci., 53, pp. 3675-3680 (2006)

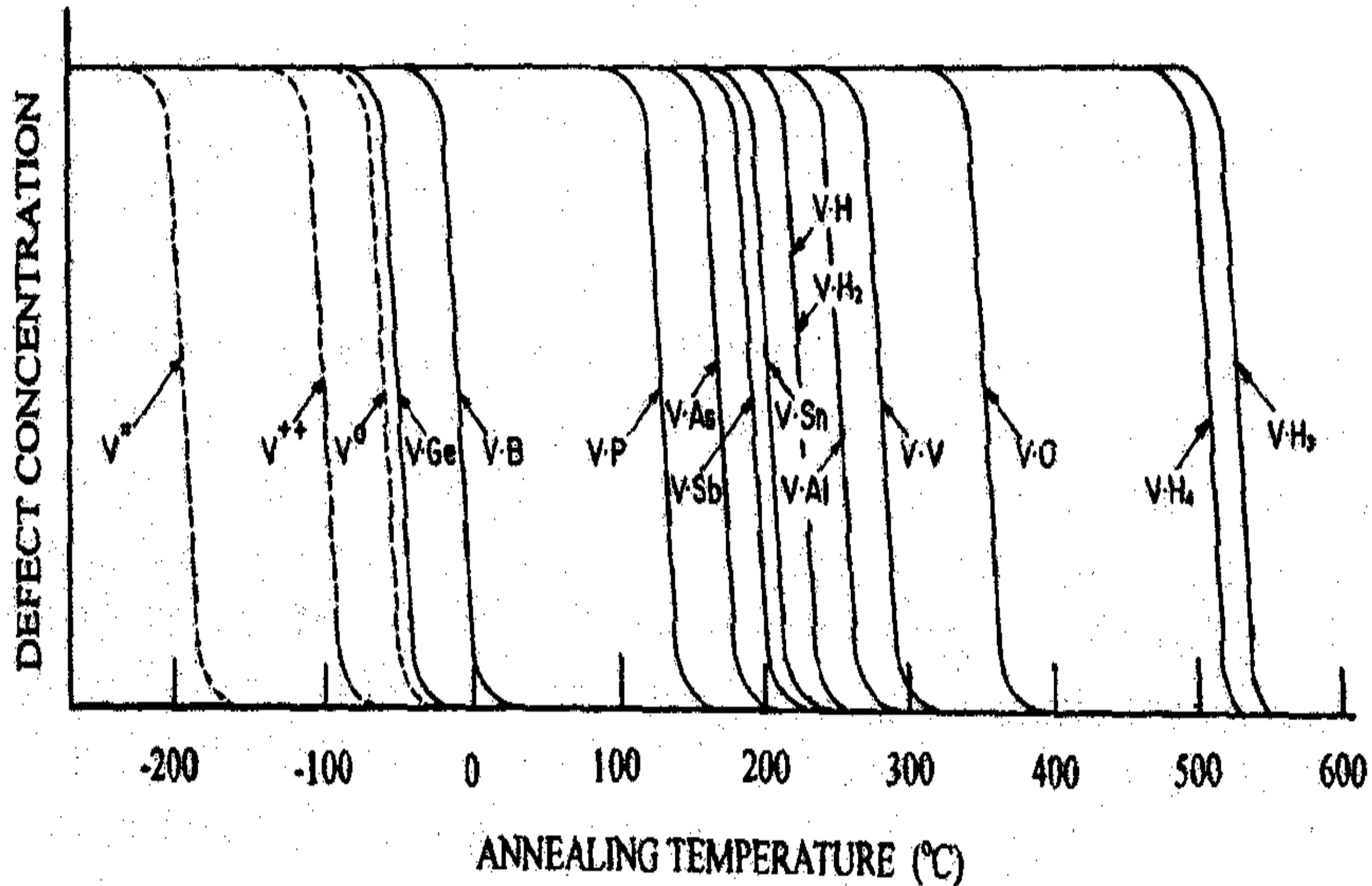
Radiation Damage

- If kinetic energy > displacement energy: formation of Frenkel pairs.
- Due to atomic displacement lattice defects are formed consisting of vacancies and/or interstitials and possible interactions of point defects with impurity atoms



- The type of stable radiation defects (RDs) depends on the irradiation temperature.
- In the first instance, the RD concentration scales with the particle fluence

Implantation Damage – Defect Stability



Schematic of vacancy and vacancy-defect pair annealing stages (~15 min isochronal) (Watkins 2000).

Displacement Damage – DLTS Traps

- **In p-type Si most important traps after RT proton irradiation are:**

  H4 (0.20 eV, VV or VVO complex)

  H5 (0.36 eV, C_sO_i or C_iC_s complex)

- **In n-type Si most important traps after RT proton irradiation are:**

  E1 (0.17 eV, VO complex)

  E2 (0.36 eV, VV complex)

  E3 (0.32 eV, VV or VP complex)

- **Isochronal and isothermal annealing can be used to study the stability of the traps (= info concerning their identity)**

Displacement Damage

Electrical parameters of the dominant radiation defects in Si stable at 300 K

Defect centre	Band gap enthalpies[a] [eV]	c_n [cm^3/s]	c_p [cm^3/s]	T Interval [K]
V-O$^{0/-}$	0.164	$1.4\text{x}10^{-8}\text{x}T^{0.5}$	$8\text{x}10^{-8}\text{x}T^{0.7}$	80-108
V-V$^{-/--}$	0.225	$1.6\text{x}10^{-12}\text{x}T^{1.4}$	$7\text{x}10^{-7}$	105-155
V-V$^{0/-}$	0.421	$5.4\text{x}10^{-9}\text{x}T^{0.4}$	$2\text{x}10^{-6}\text{x}T^{-0.3}$	182-266
V-V$^{+/0}$	0.194	$\gg c_p$	$2.1\text{x}10^{-9}\text{x}T^{0.2}$	104-146
C_iO_i	0.339	$5.1\text{x}10^{-23}\text{x}T^{5.2}$	$1.2\text{x}10^{-10}\text{x}T^{0.61}$	160-238

c_n electron capture rate, c_p hole capture rate, T temperature
[a]The trap energy E_T is related to the enthalpy ΔH and entropy ΔS through $E_c - E_T = \Delta H_T - T\Delta S_T$

Low Temperature Electronics

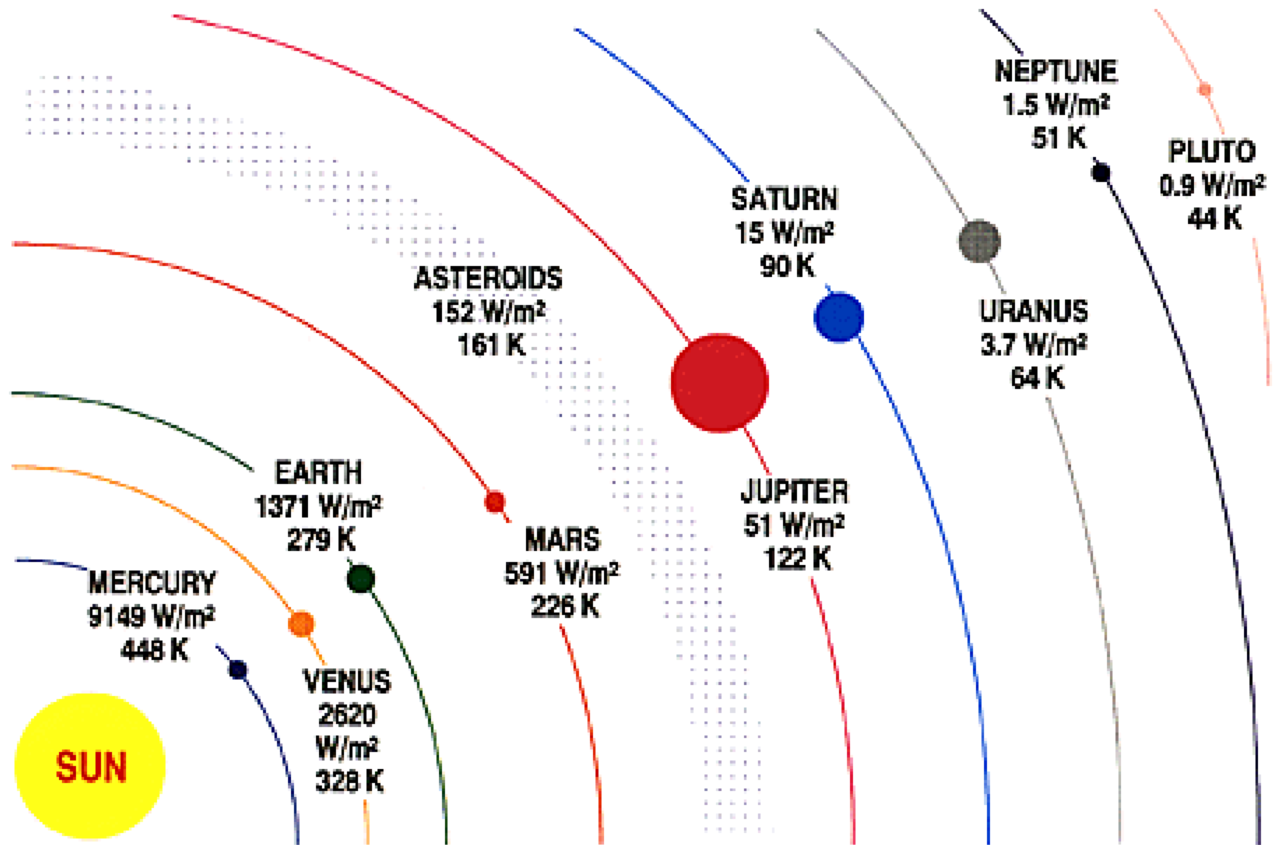
Low temperature Electronics

- **Liquid Nitrogen Temperature Range (T=77 K): potential for commercial applications (supercomputers) and scientific/space instrumentation (Large Hadron Collider; Charge- Coupled Devices)**

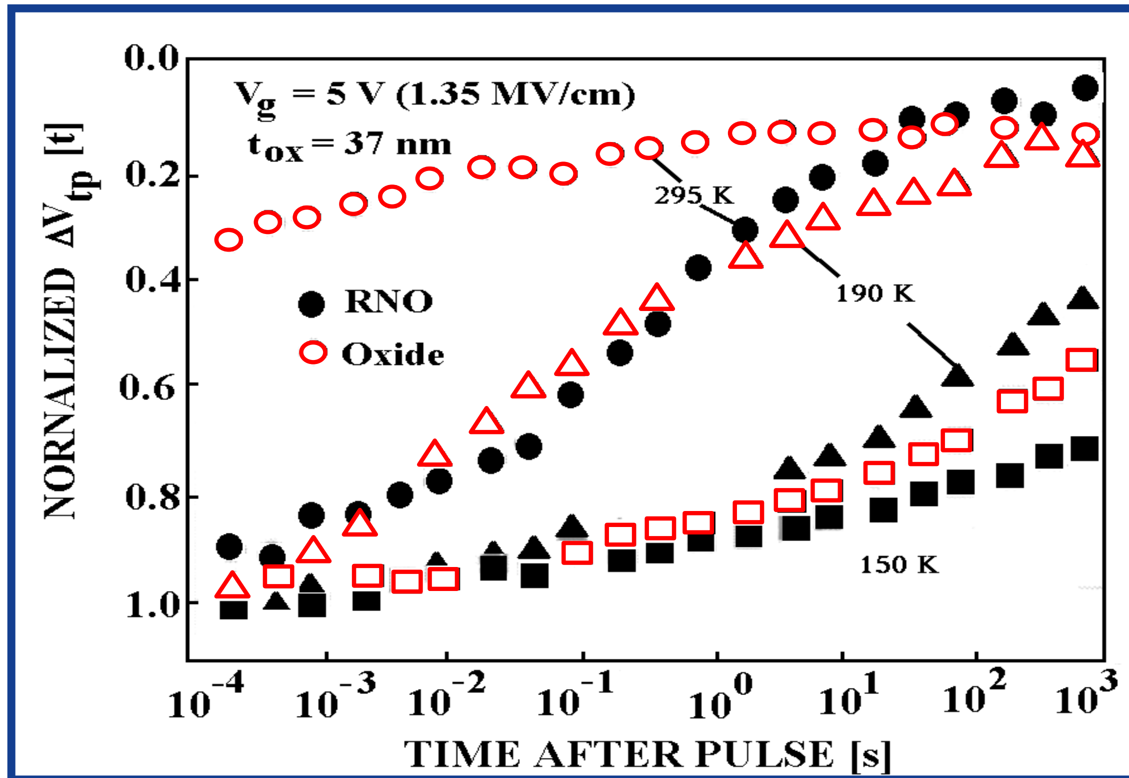
- **Liquid Helium Temperature Range (T=4.2 K): satellite communications and far-infrared focal plane arrays (ISO; HERSCHEL)**

- **mK range: astrophysical applications (bolometers)**

Temperature in Space Missions



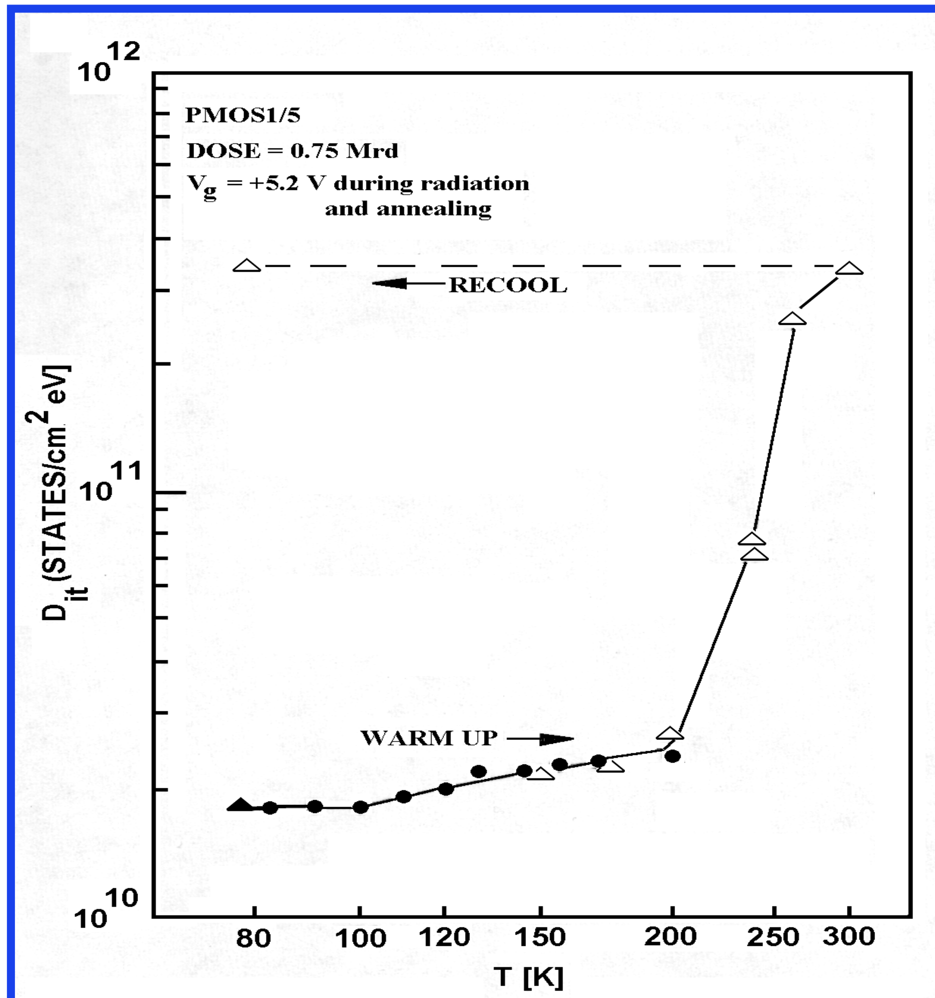
Ionization Damage – Threshold Voltage Shift



At or below 150 K the trapped holes in the oxide are frozen in. Hardly no recovery takes place

➔ the degradation of the flat-band or threshold voltage is higher than at room temperature.

Ionization Damage – Interface Traps



After 77 K total dose irradiation, no interface traps are formed

➔ absence of the rebound effect in V_T.

Low Temperature Electronics

- Single Event Upset SEU

band gap for lower T, which reduces the numbers of generated e-h pairs.

- Radiation-induced Latch up SEL

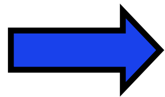
gain (parasitic) bipolar reduces upon cooling. Some studies have pointed out an optimum operation temperature (~120 K). Will strongly depend on technological details.

Low Temperature Electronics - Summary

- The radiation response of CMOS components shows a pronounced temperature dependence, e.g., at cryogenic temperatures, no interface states are formed.

- Total-dose damage should be worst case at cryogenic temperatures (no annealing), while the opposite in principle holds for displacement damage.

- At cryogenic temperatures, specific effects (kink/ hysteresis) may occur.

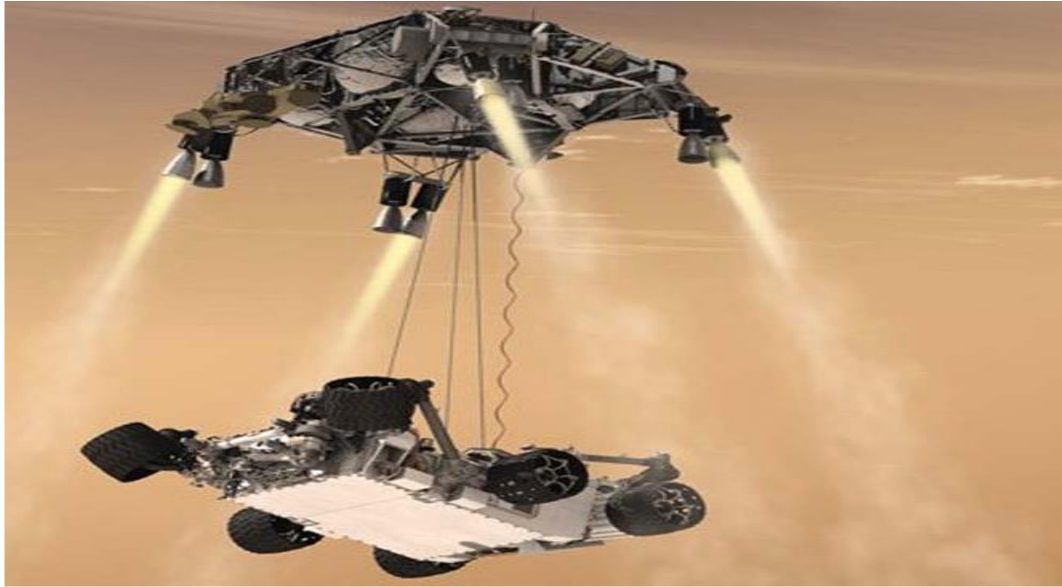


Importance of cryogenic radiation testing

Radiation Hardness Microelectronic Components

Motivation Advanced Microelectronics Components for Space

COTS important for Space Applications



Moore's Law

Integrated Circuit Complexity

Transistors Per Die

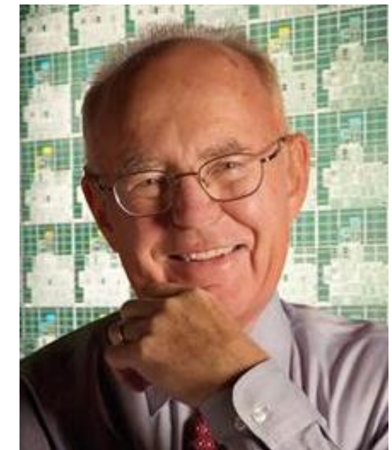
10^{10}, 10^9, 10^8, 10^7, 10^6, 10^5, 10^4, 10^3, 10^2, 10^1, 10^0

1965 Actual Data
MOS Arrays
MOS Logic 1975 Actual Data
1975 Projection
Memory
Microprocessor

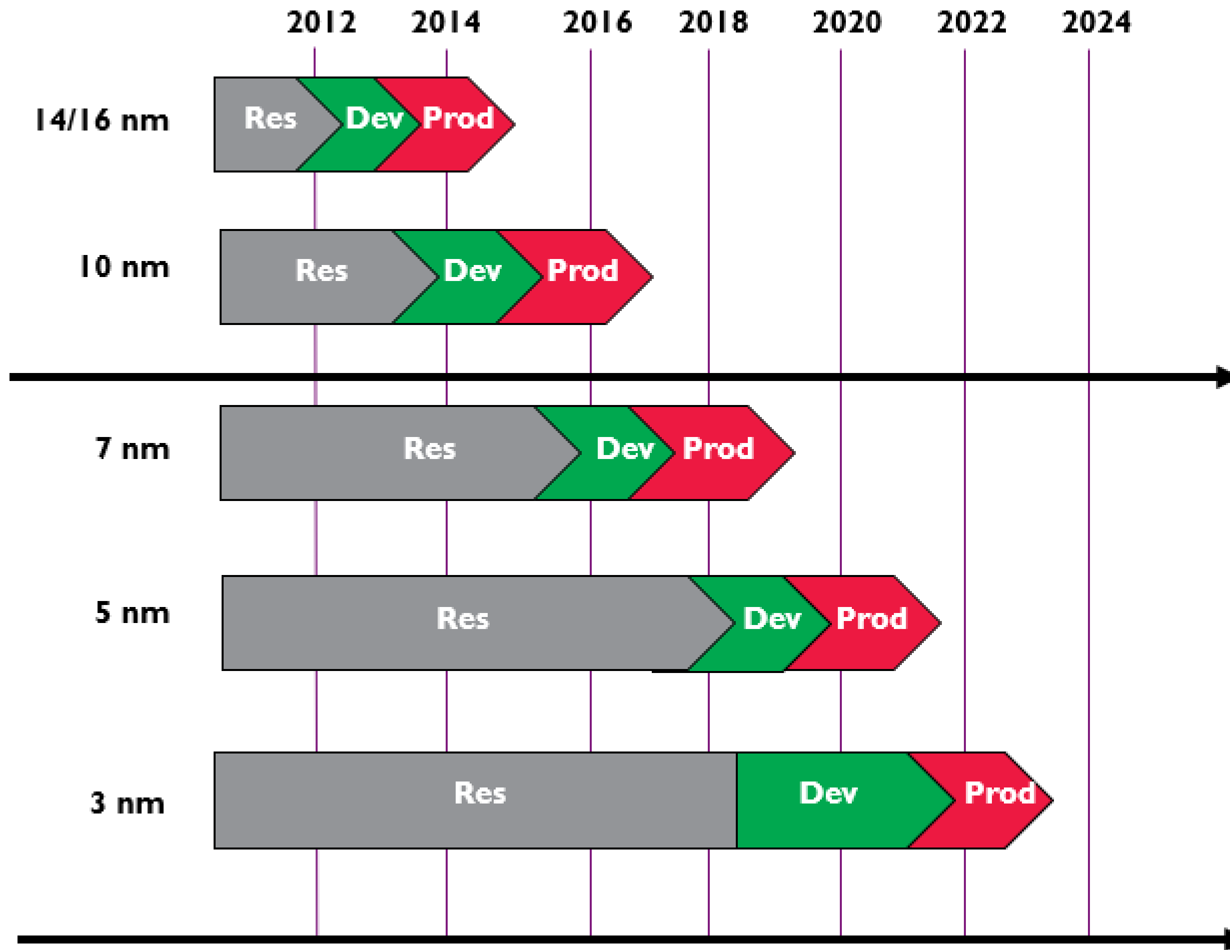
1K, 4K, 16K, 64K, 256K, 1M, 4M, 16M, 64M, 128M, 256M, 512M, 1G, 2G, 4G

4004, 8080, 8086, 80286, i386™, i486™, Pentium®, Pentium® II, Pentium® III, Pentium® 4, Itanium™

1960, 1965, 1970, 1975, 1980, 1985, 1990, 1995, 2000, 2005, 2010

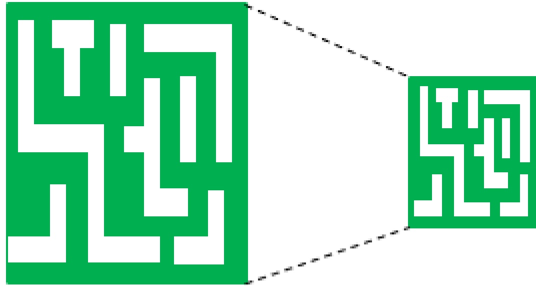


Research – Development - Production
Scaling Roadmap

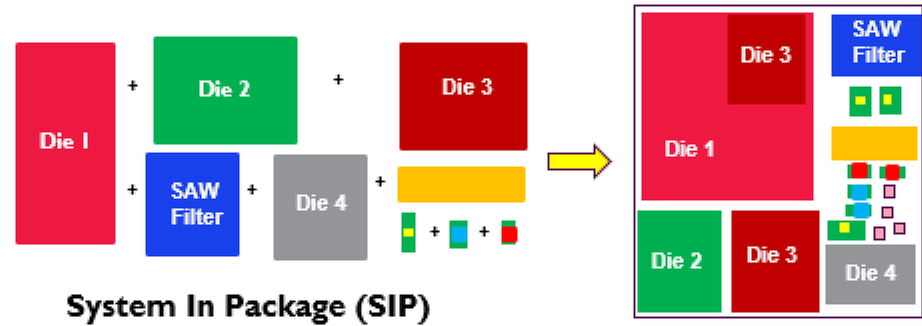


Scaling approaches to Cope with Moore's Law

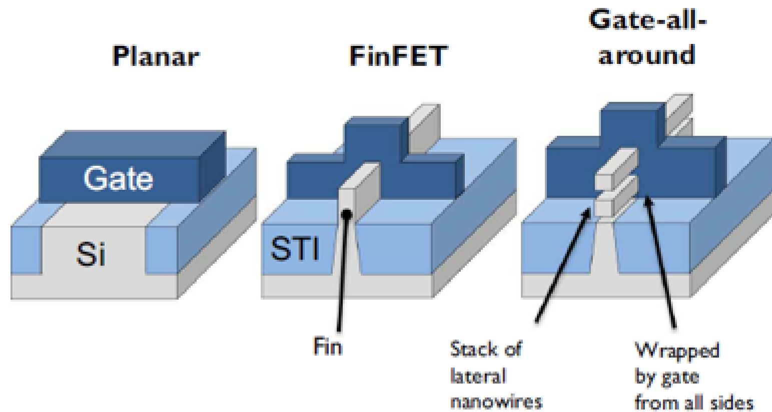
Geometric Scaling
2D scaling through lithography



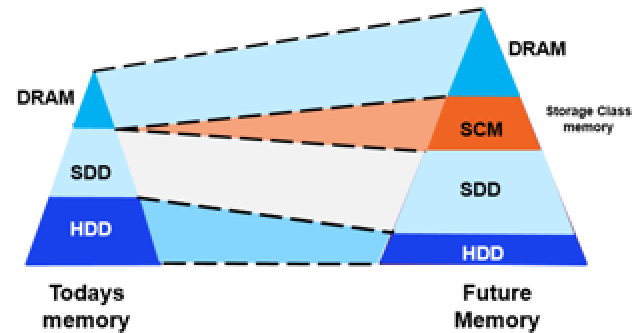
Circuit Scaling
System In Package + Advanced Packaging



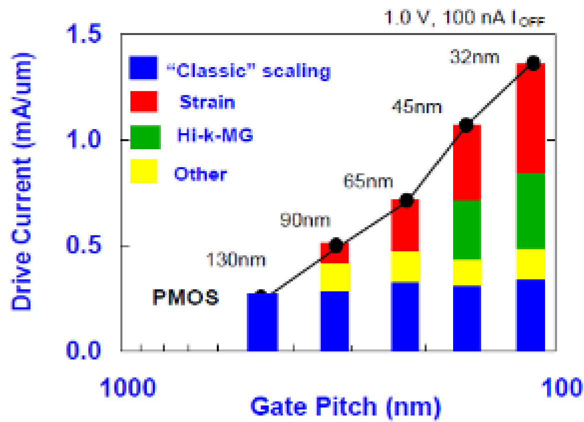
Material/Device Scaling
2D scaling through lithography



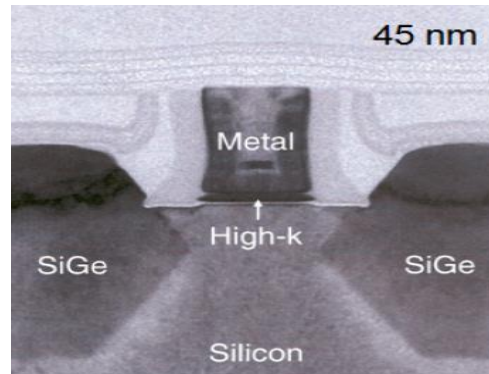
Architecture Scaling
Solutions optimization



Process Innovation and Process Complexity



K. Mistry *et al.*, *Techn. Dig. IEDM*, 274 (2007)

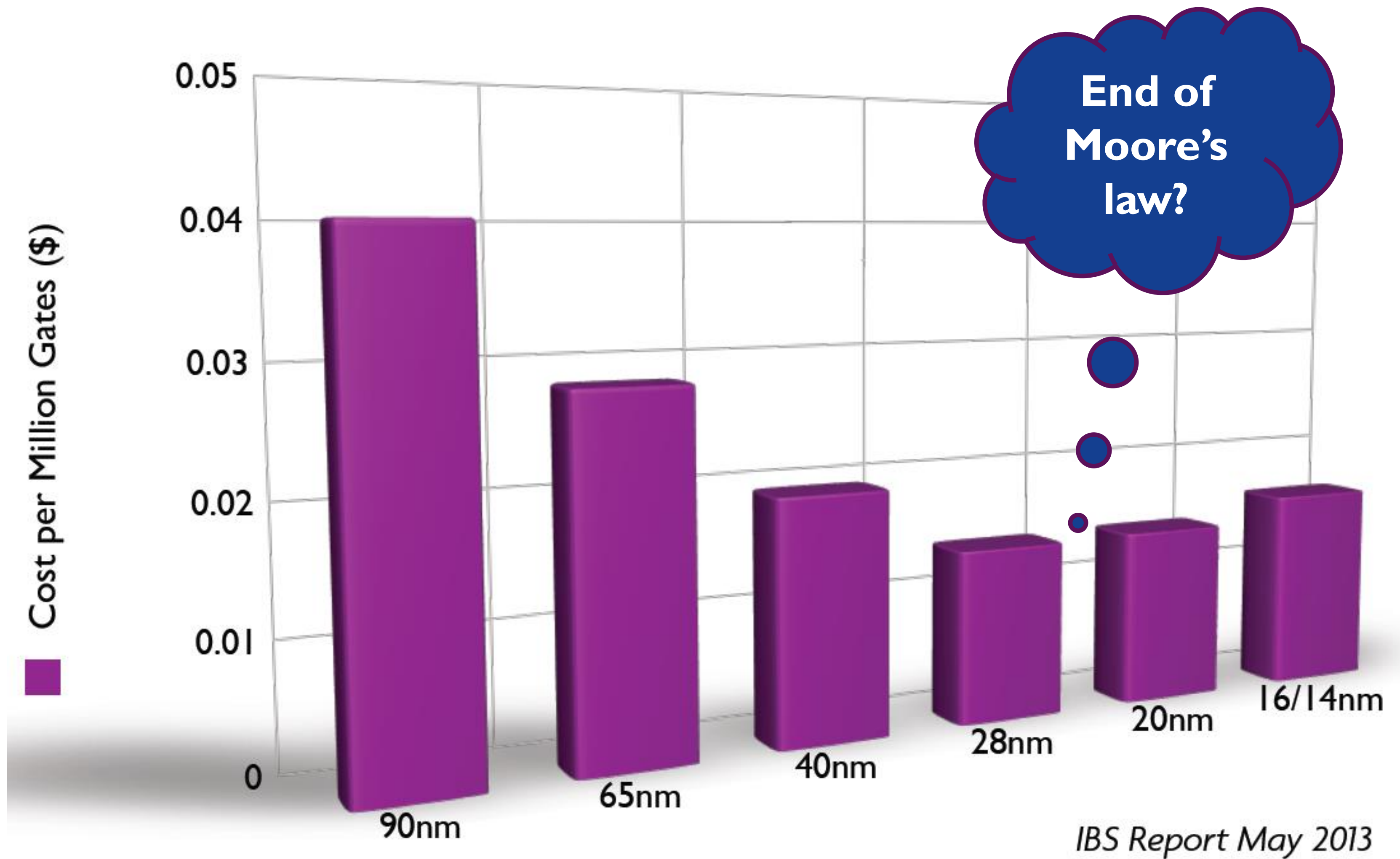


Performance

	350	250	180/130	90	65 /45	45/32	28/20	14/beyond
BEOL	Al Wires	FTEOS ILD	FTEOS ILD, Cu Barriers, Cu wiring	ILD Cu caps	CPI, Low K ILD, CoWP cap	Low-K ESL, Ultra Low-K, ULK Cap, Eless Cu	TSVs, AIR GAP, Porous LK, Cu Alloys, Electroless Cu	Sel Metal caps, Porous LK, New Cu BM, Cu Alloys, Eless Cu
Contacts	$TiSi_2$	CVD W, MOCVD TiN, $CoSi_2$		ALD W, NiPtSi			Cu Contact, Dual Si_2	MIS, Dual Si_2
Device						High K, Metal Gate, Gate First	ALD Metals, Replacement Metal Gate	Fin FET, Multiple EWF, Si-50%Ge, Ge MOS
Channel	Bulk Si		SOI	Si Strain	Stress Liner, Si-Ge	Si orientation	Stress Liner, Si-C	SiGe channel, Si-P

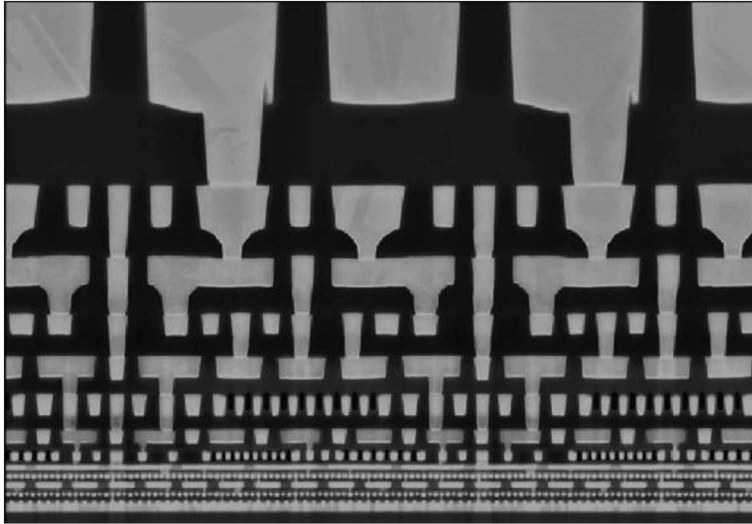
Technology Node

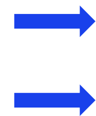
Cost per Gate



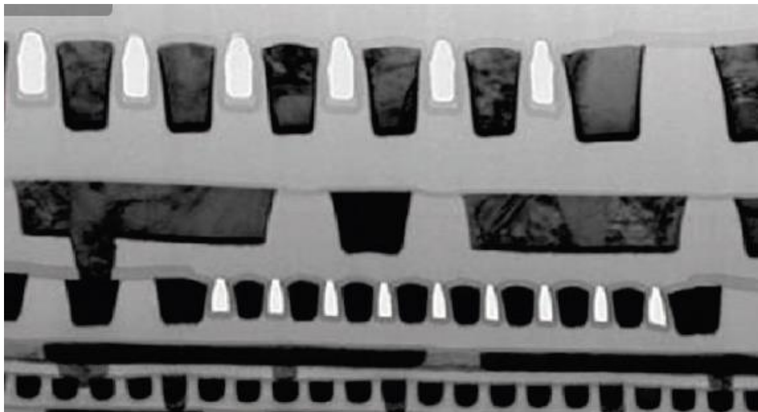
14 nm Intel Process

Intel 14 nm – 13 metal layers





Metal	Process	Dielectric	Pitch (nm)	Layer Thx (nm)	Metal Thx (nm)	AR
0	PD SAV	LK CDO	56	70	40	1.4
1	PD SAV	ULK CDO	70	81	42	1.2
2	PD SAV	ULK CDO	52	73	40	1.5
3	PD SAV	ULK CDO	56	76	37	1.3
4	SAV	Air Gap	80	145	75	1.9
5	SAV	ULK CDO	100	210	110	2.2
6	SAV	Air Gap	160	310	180	2.3
7	SAV	ULK CDO	160	380	200	2.5
8	SAV	ULK CDO	160	400	200	2.5
9	Via First	LK CDO	252	540	260	2.1
10	Via First	LK CDO	252	675	375	3.0
11	Via First	SiO2	1080	1770	1080	2.0
12	Plate Up	polymer	14000	~	6000	1.3



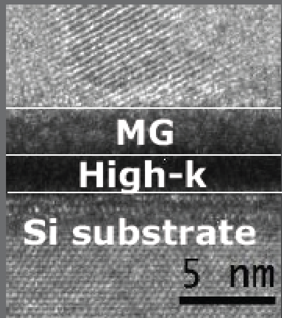
Airgaps in M4 and M6

SAV: Self-aligned via
CDO: Carbon doped oxide

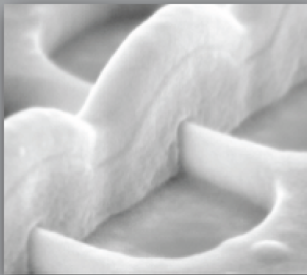
Trends to Increase Device Performance

MATERIAL DEVICE MATERIAL DEVICE MATERIAL

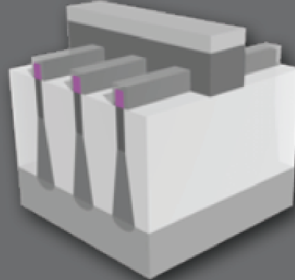
METAL GATE HIGH K



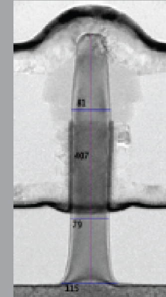
FINFET



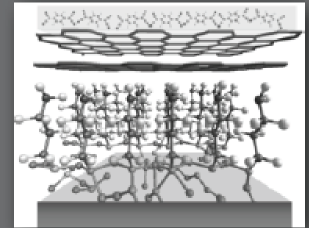
HIGH MOBILITY CHANNELS



NANOWIRE/ TUNNEL FETs

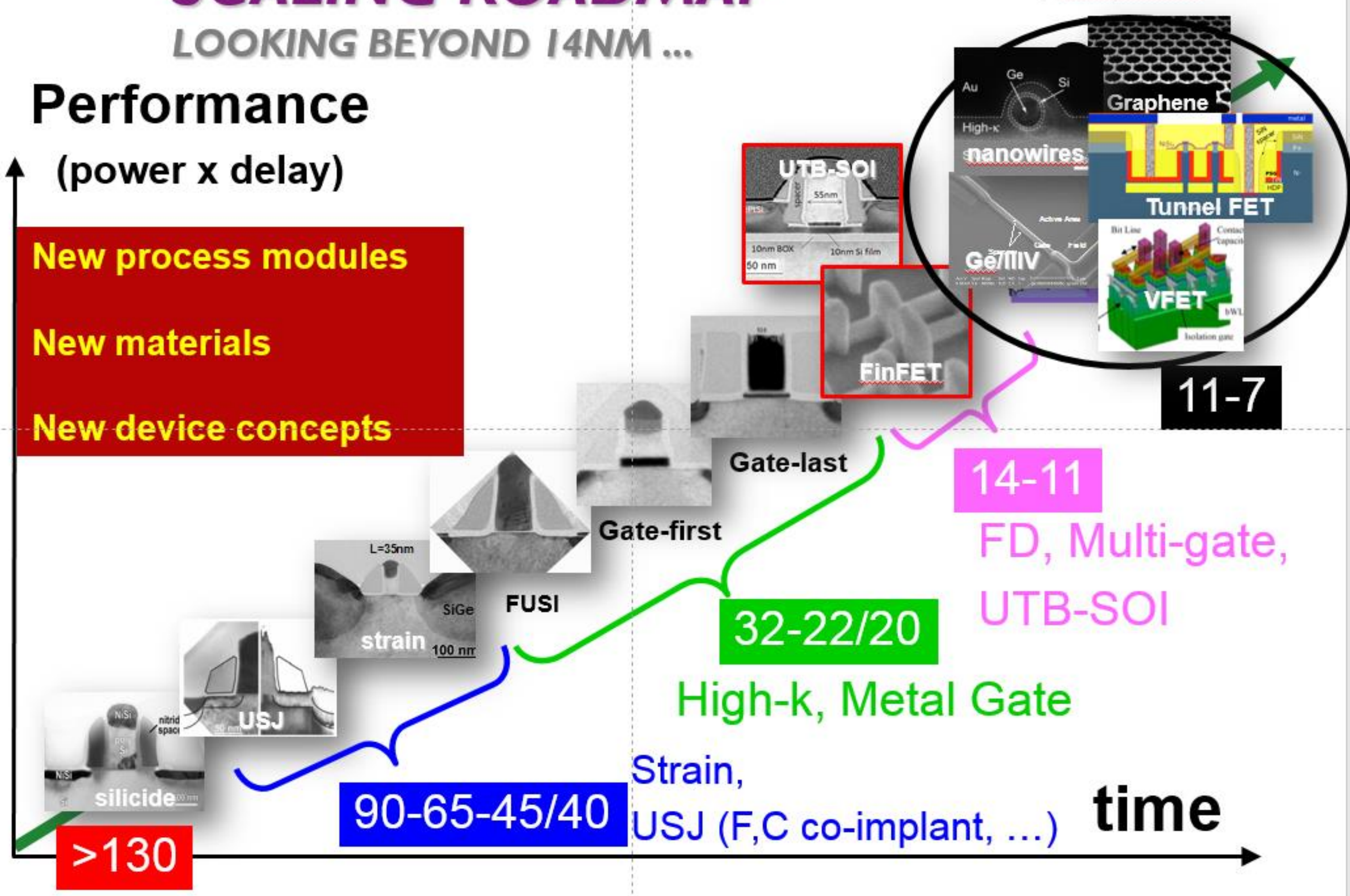


2D MATERIALS

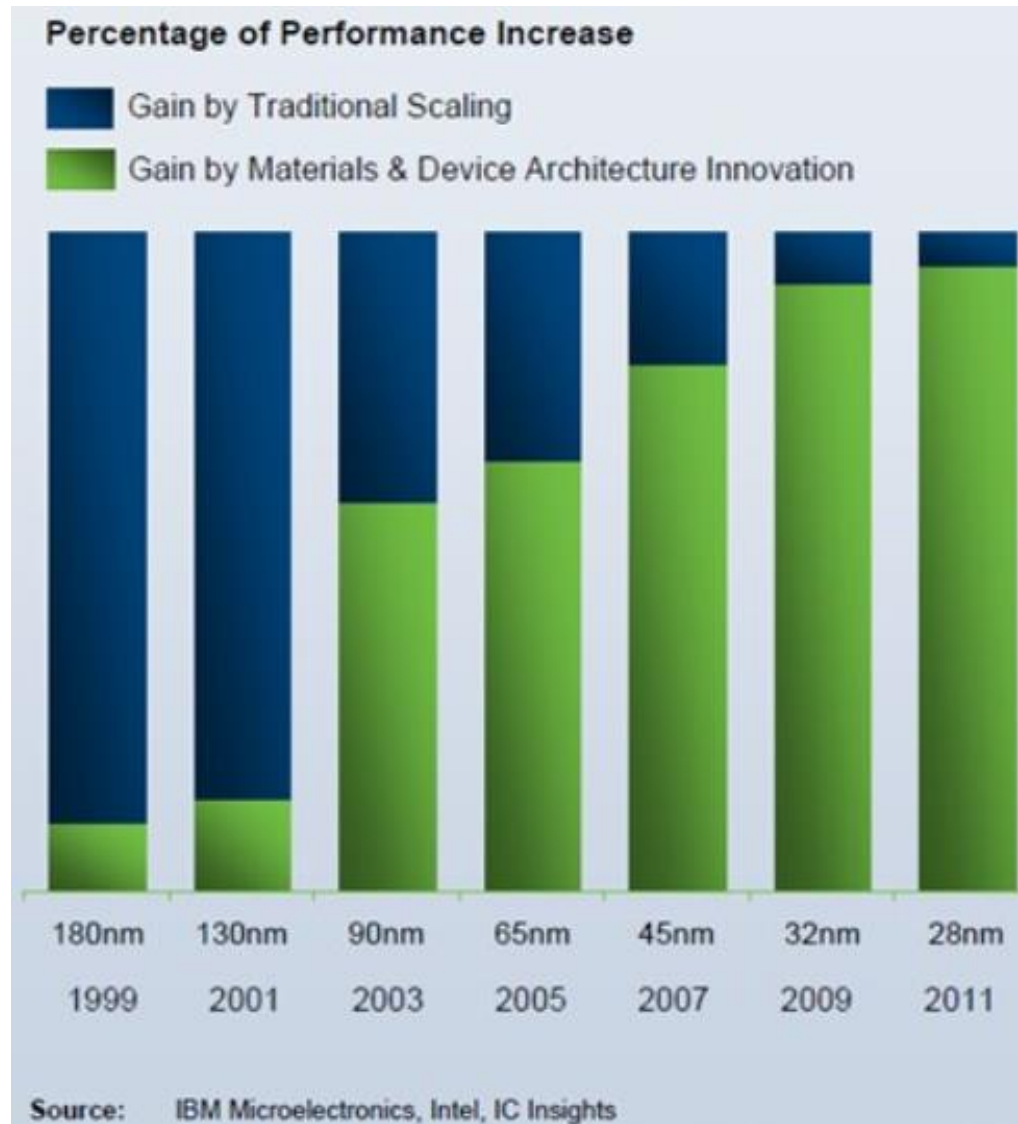


45nm → 32/28nm → 22/20nm → 14nm → 10nm → 7nm → 5nm → ...

Tech Node


SCALING ROADMAP
LOOKING BEYOND 14NM …
Performance
(power x delay)
Ge/III-V, VFET, TFET,
NW, Graphene…
New process modules
New materials
New device concepts
Graphene
nanowires
Tunnel FET
Ge/III-V
VFET
UTB-SOI
FinFET
11-7
Gate-last
Gate-first
FUSI
strain
USJ
silicide
14-11
FD, Multi-gate,
UTB-SOI
32-22/20
High-k, Metal Gate
90-65-45/40
Strain,
USJ (F,C co-implant, …)
time
>130

Scaling– Performance Improvement



Gate Dielectrics

Gate Dielectrics – Replacement SiO_2

Candidates

● Gas or liquid at 1000 K

Unstable at Si interface

○ Radio active

① $Si + MO_X$ $M + SiO_2$

② $Si + MO_X$ $MSi_X + SiO_2$

③ $Si + MO_X$ $M + MSi_XO_Y$

● H ● He

Li Be ● B ● C ● N ● O ● F ● Ne

① Na Mg Al Si ● P ● S ● Cl ● Ar

K Ca Sc ② Ti ① V ① Cr ① Mn ① Fc ① Co ① Ni ① Cu ① Zn ① Ga ① Ge ● As ● Se ● Br ● Kr

● Rh Sr Y Zr ① Nb ① Mo Tc ① Ru ① Rb ① Pd ● Ag ① Cd ① In ① Sn ① Sb ① Te ● I ● Xe

● Cs ③ Ba ★ Hf ① Ta ① W ① Re ① Os ① Ir ● Pt ● Au ● Hg ● Tl ① Pb ① Bi ○ Po ○ At ○ Rn

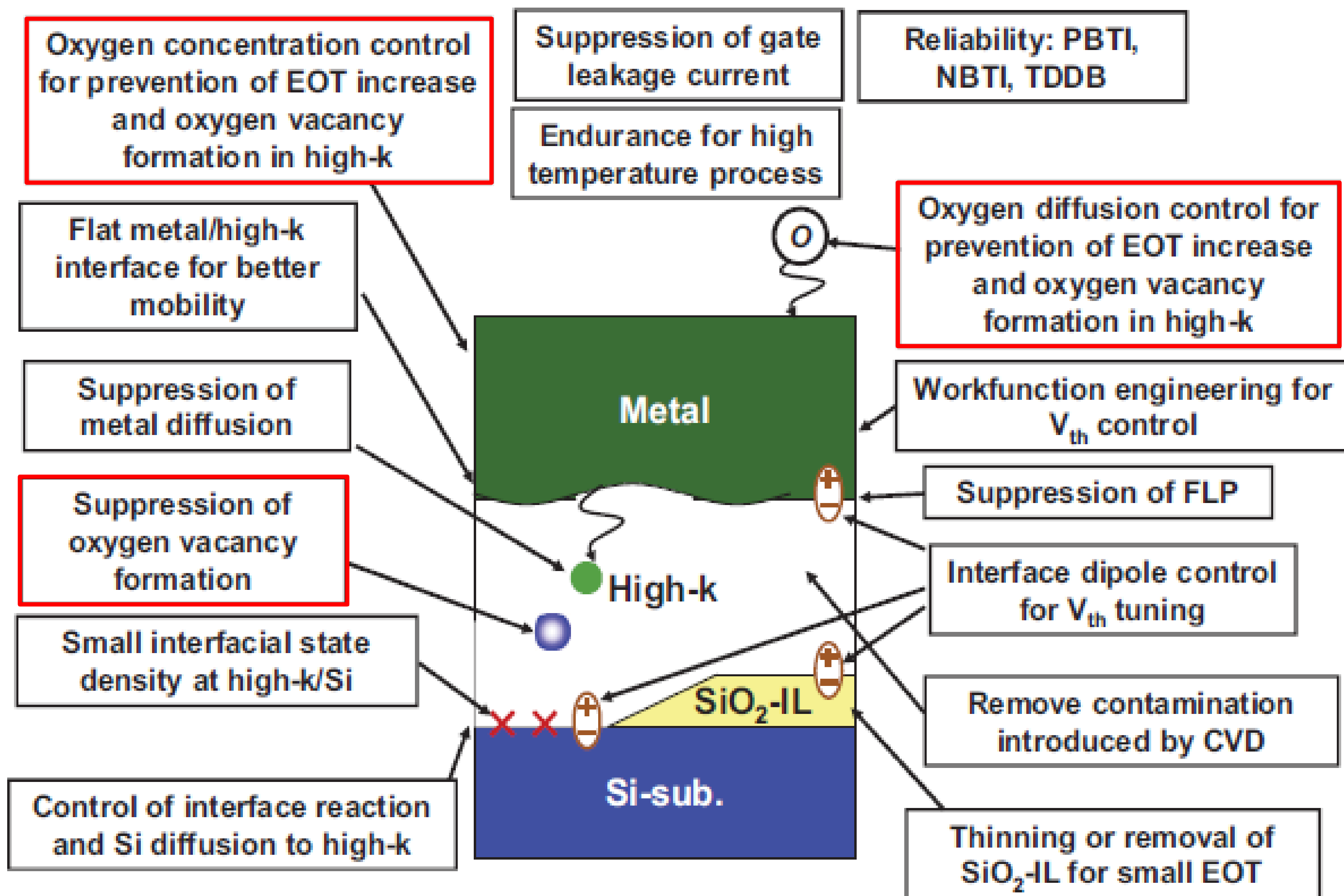
○ Fr ○ Ra ☆ ○ Rf ○ Ha ○ Sg ○ Ns ○ Hs ○ Mt

★ La Ce Pr Nd ○ Pm Sm Eu Gd Tb Dy Ho Er Tm Yb Lu

☆ ○ Ac ○ Th ○ Pa ○ U ○ Np ○ Pu ○ Am ○ Cm ○ Bk ○ Cf ○ Es ○ Fm ○ Md ○ No ○ Lr

- Gate leakage due to tunneling: 3 nm
- Increased κ-factor
- Defects:
  - Bulk
  - Interface

Challenges Related to Gate Dielectrics

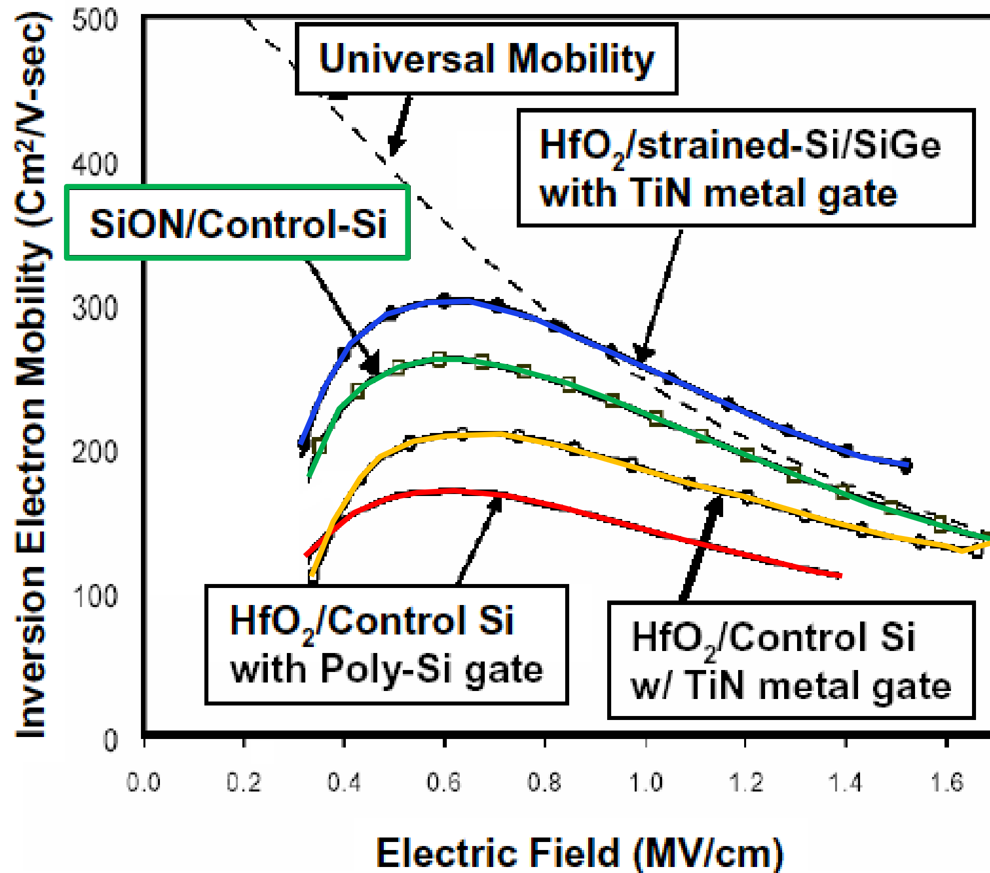


H. Iwai, Solid-State Electron., 112, 56 (2015)

Strain Engineering

Scaling Technology

➢Use of high-κ dielectrics + metal gate + strained Si

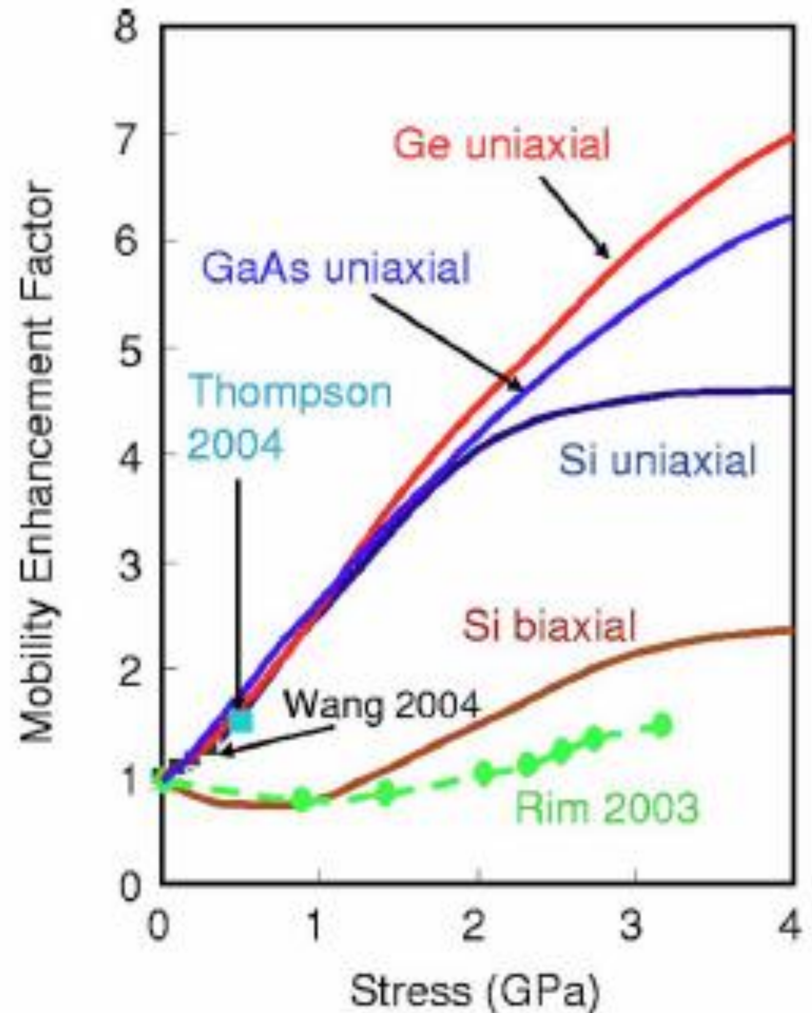


35% increase for strained Si/SiGe

S. Datta et al., IEDM 2003, p. 653

Strain Engineering

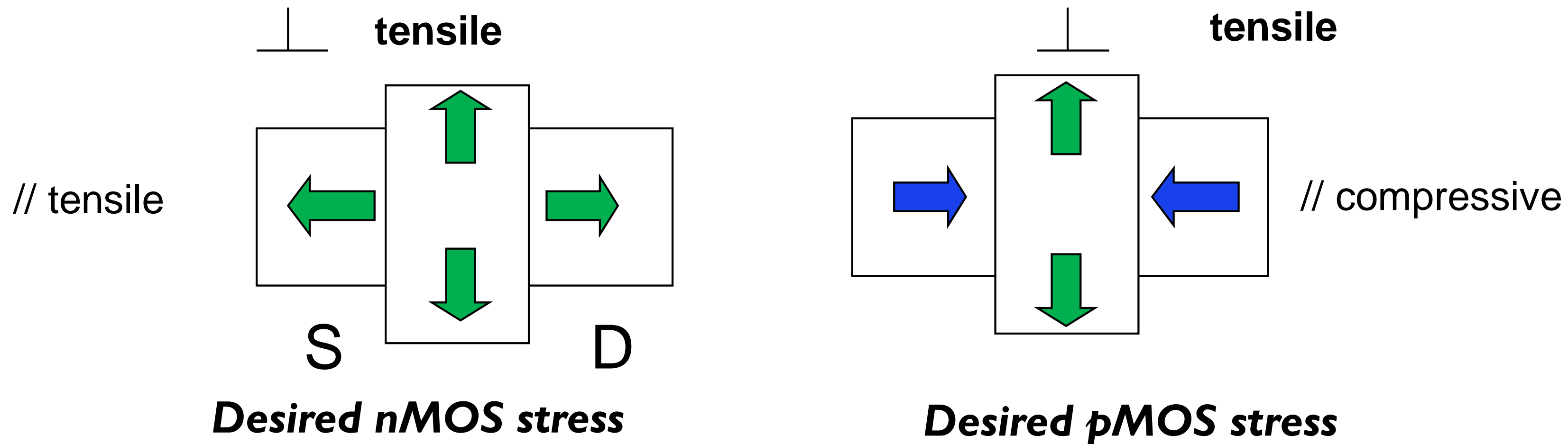
Hole mobility enhancement factor of Si, Ge, and GaAs as a function of stress. The dashed line is the experimental observation of hole mobility enhancement versus biaxial stress.

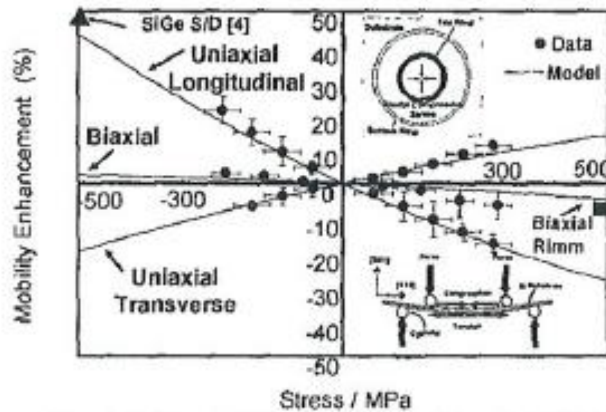


Y. Sun, S.E. Thompson and T. Nishida, J. Appl. Phys. 101, 104503 (2007).

Strain Engineering

Strain in MOSFETs

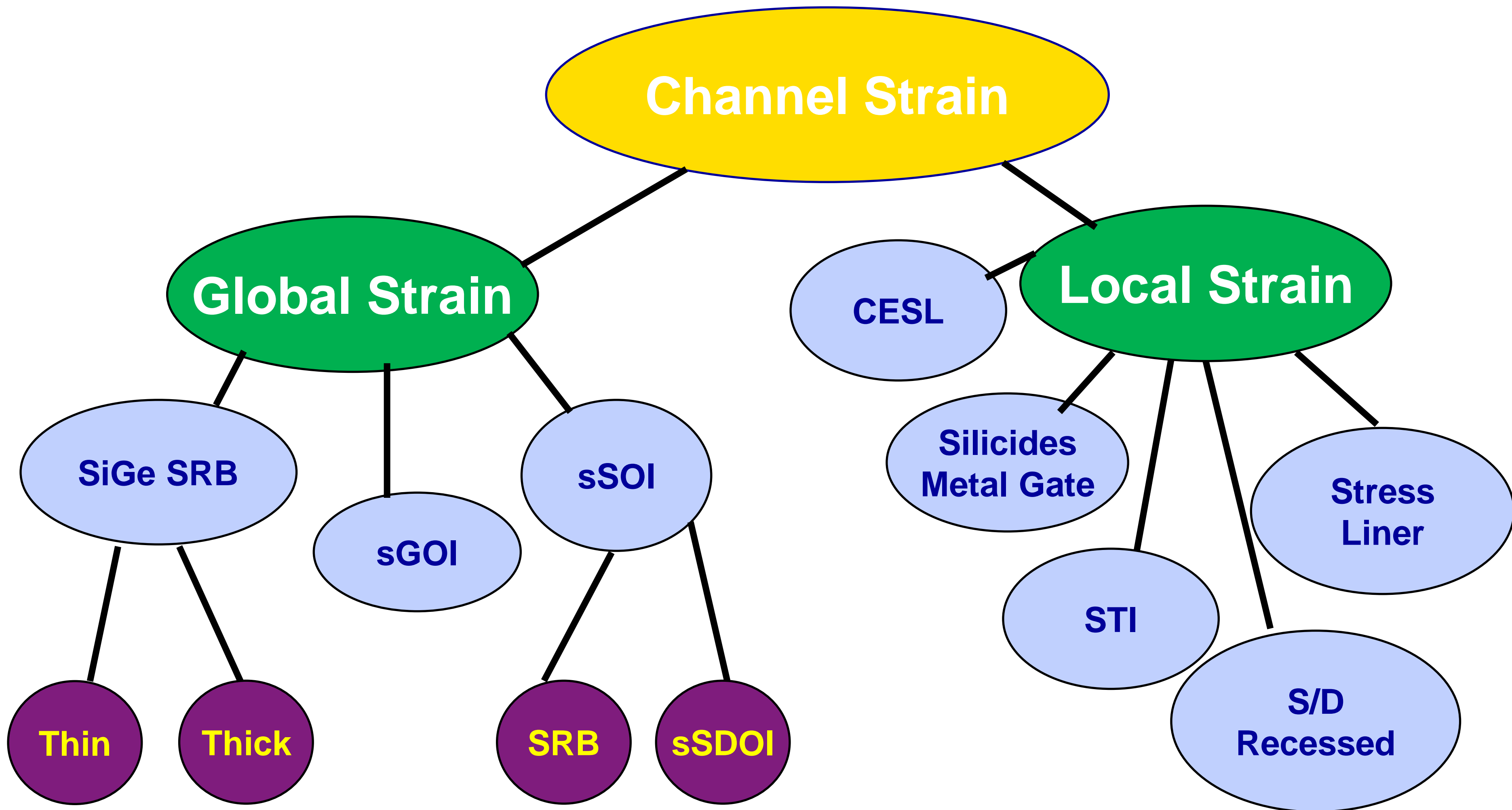




Enhanced mobility vs. stress induced via wafer bending: biaxial and longitudinal and transverse uniaxial stress.

S.E. Thompson, G. Sun, K. Wu, J. Lim and T. Nishida, IEDM Tech. Dig. p. 221 (2004).

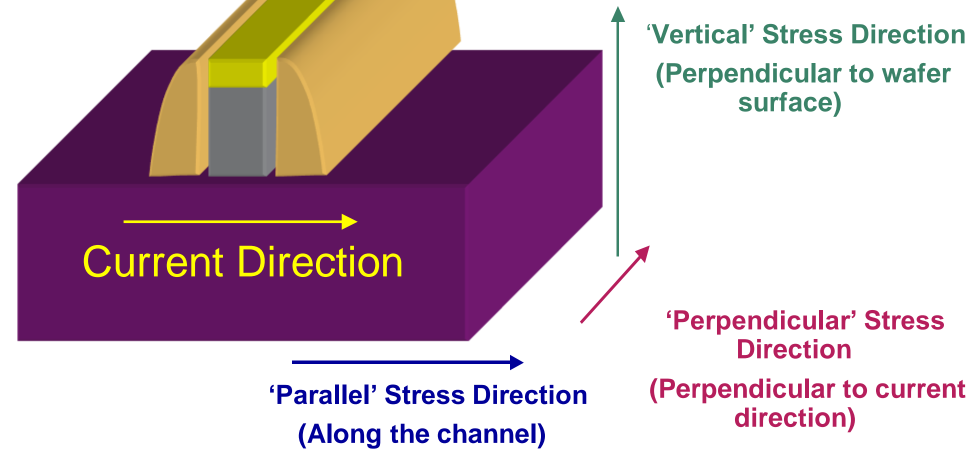
Strain Engineering Approaches



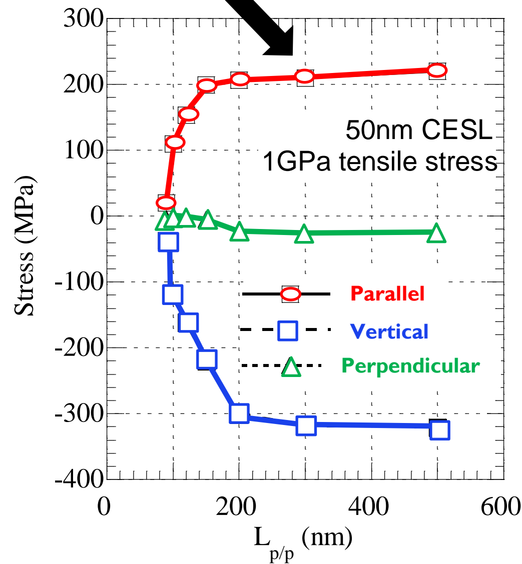
Local stressors

CESL and SiGe S/D:

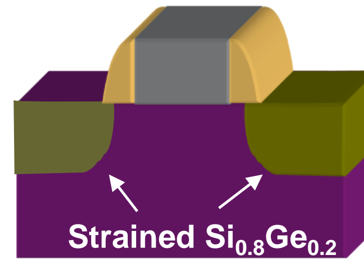
opposite behavior for induced stress

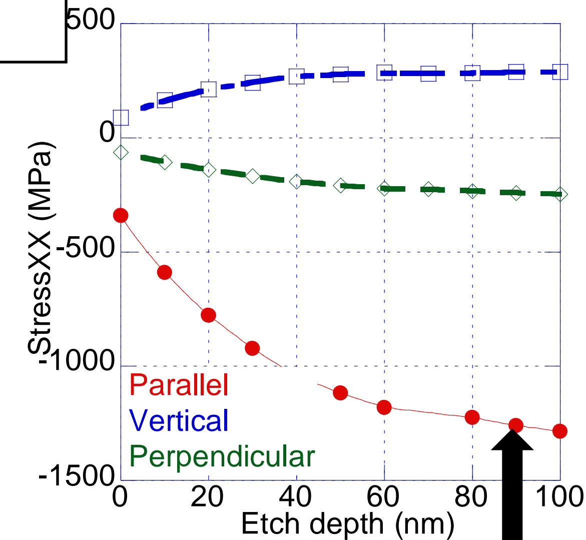


CESL



SiGe S/D





Dual CESL Stressor Process Implementation

CMOS flow implementation

Tensile

Compressive

PECVD 1 400ºC 16 % 800

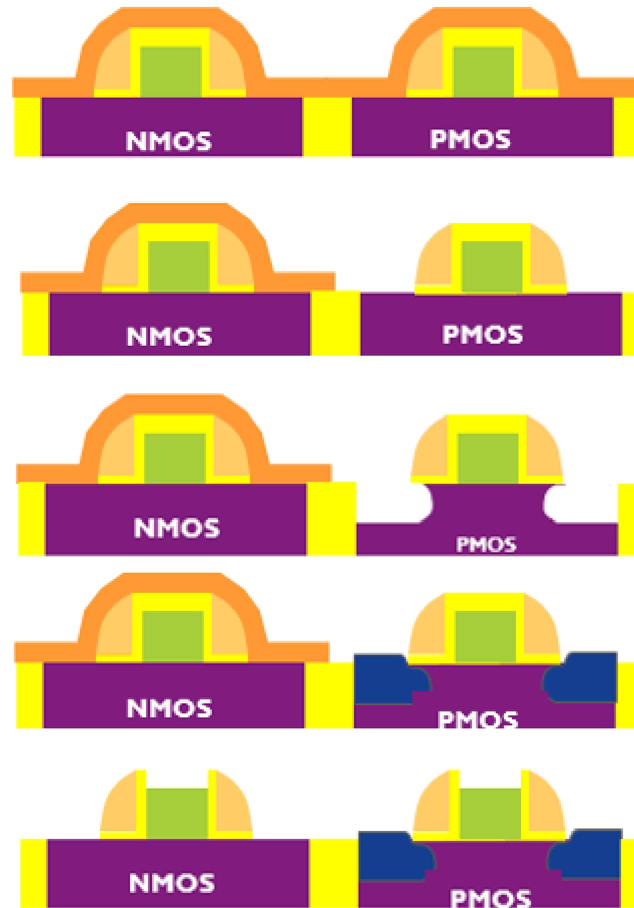
PECVD 2 400ºC 13 % -800

Dual Stressor Process Implementation

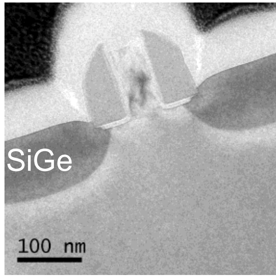
CMOS flow implementation

Tensile
CESL

compressive
Embedded S/D

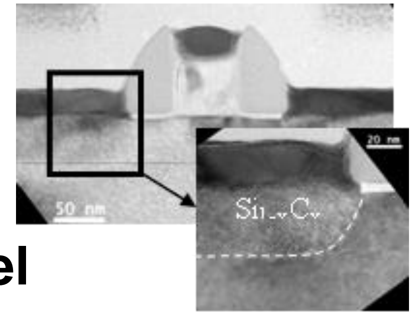


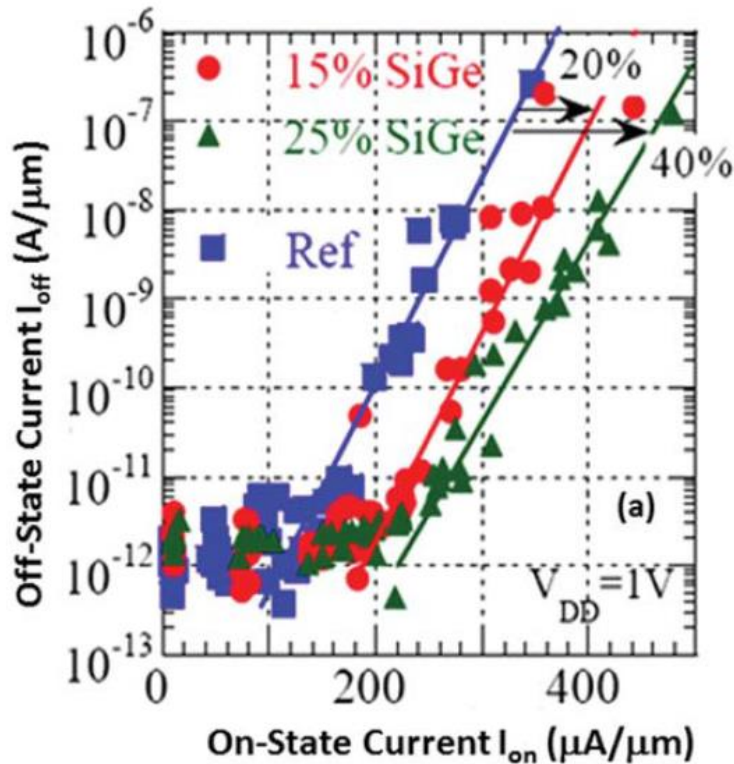
Strain Engineering

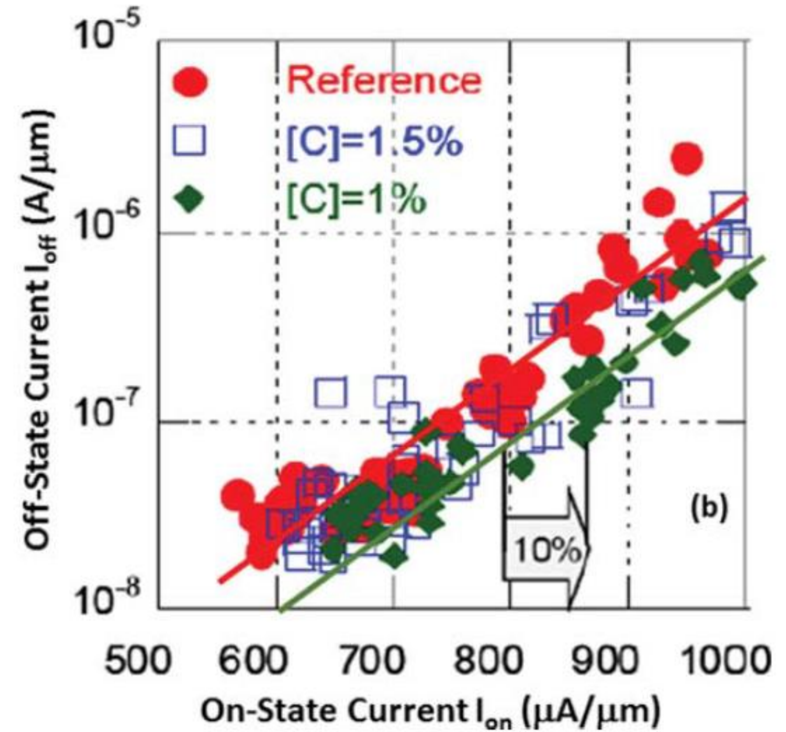


SiGe S/D
p-channel

SiC S/D
n-channel

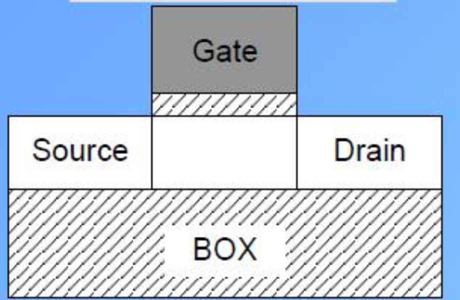


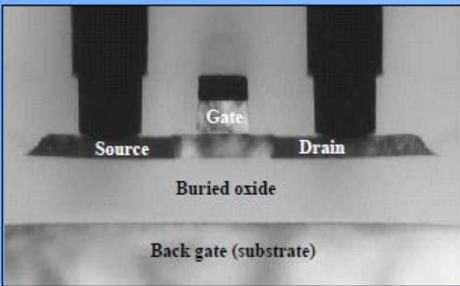


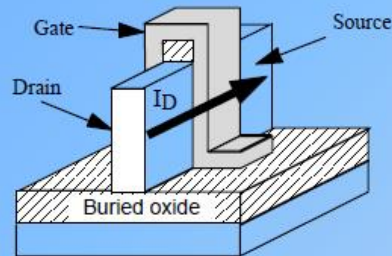


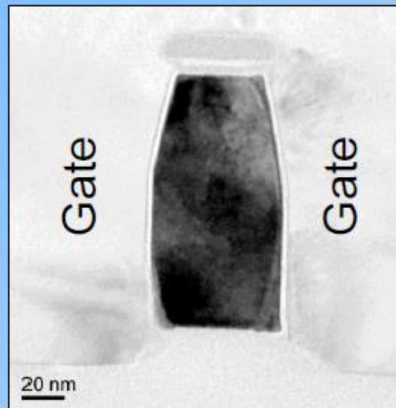
Multiple Gate Devices

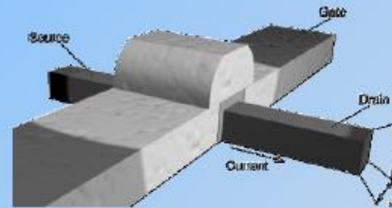
"1 Gate" → "2 Gates" → "3 Gates" → "Gate-all-Around"

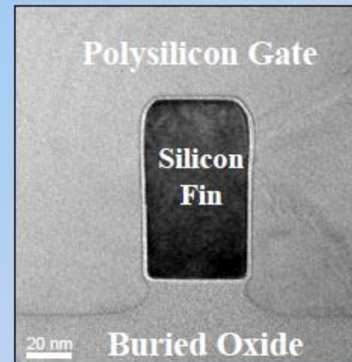


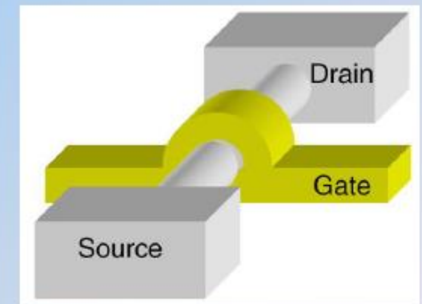


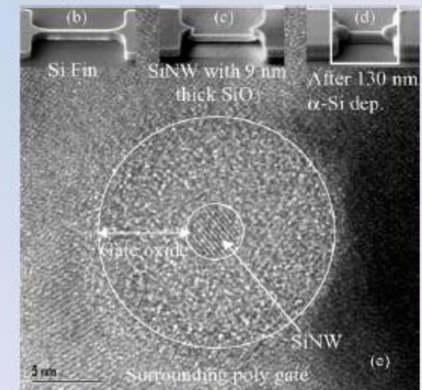






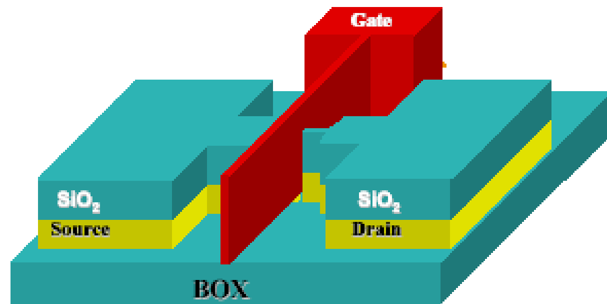




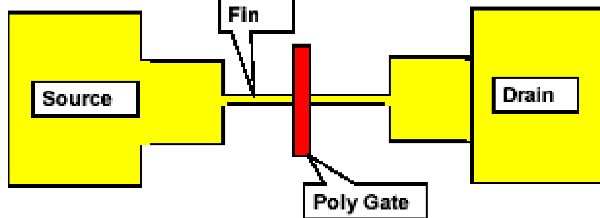


* Jean-Pierre Colinge

FinFET on SOI or Bulk

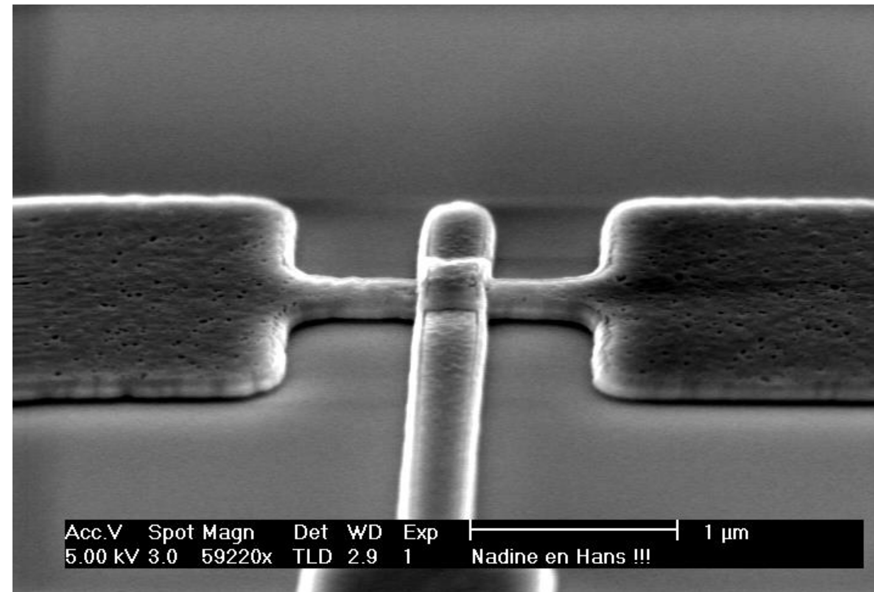


a. FinFET Cross Section



b. FinFET Top View

FinFET



Aim

DISCUSS THE RADIATION PERFORMANCE OF DIFFERENT STATE-OF-THE-ART DEVICES

SOI DEVICES AND BULK FINFETs

UTBOX DEVICES

TUNNELFETs

RESISTIVE MEMORIES

SiGe DEVICES

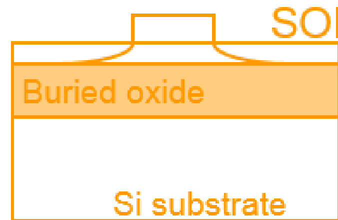
Ge-BASED TECHNOLOGIES

Radiation Hardness Fully Depleted SOI Devices

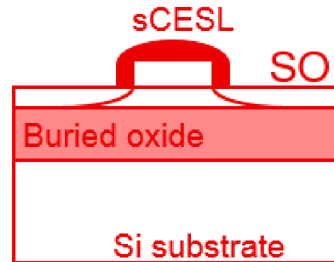
Fully Depleted SOI Technology

65 nm Fully Depleted Silicon On Insulator technology irradiated with 60 MeV protons at 5×10^{11} p/cm^2

SOI



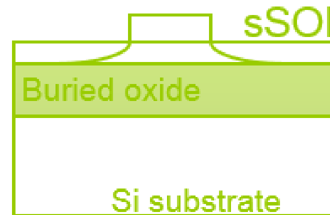
SOI + 100 nm sCESL



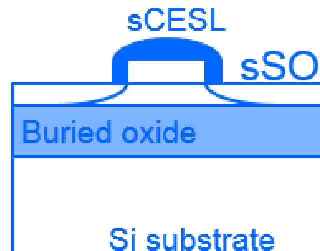
sSOI

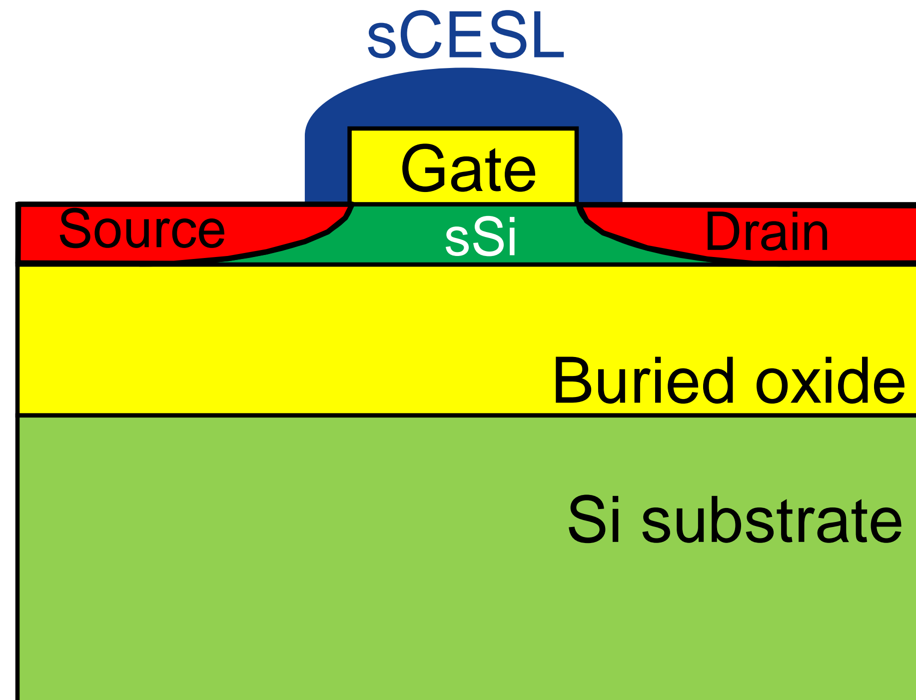
(global t-stressed SOI

1,5- 2 GPa)



sSOI + 100 nm sCESL

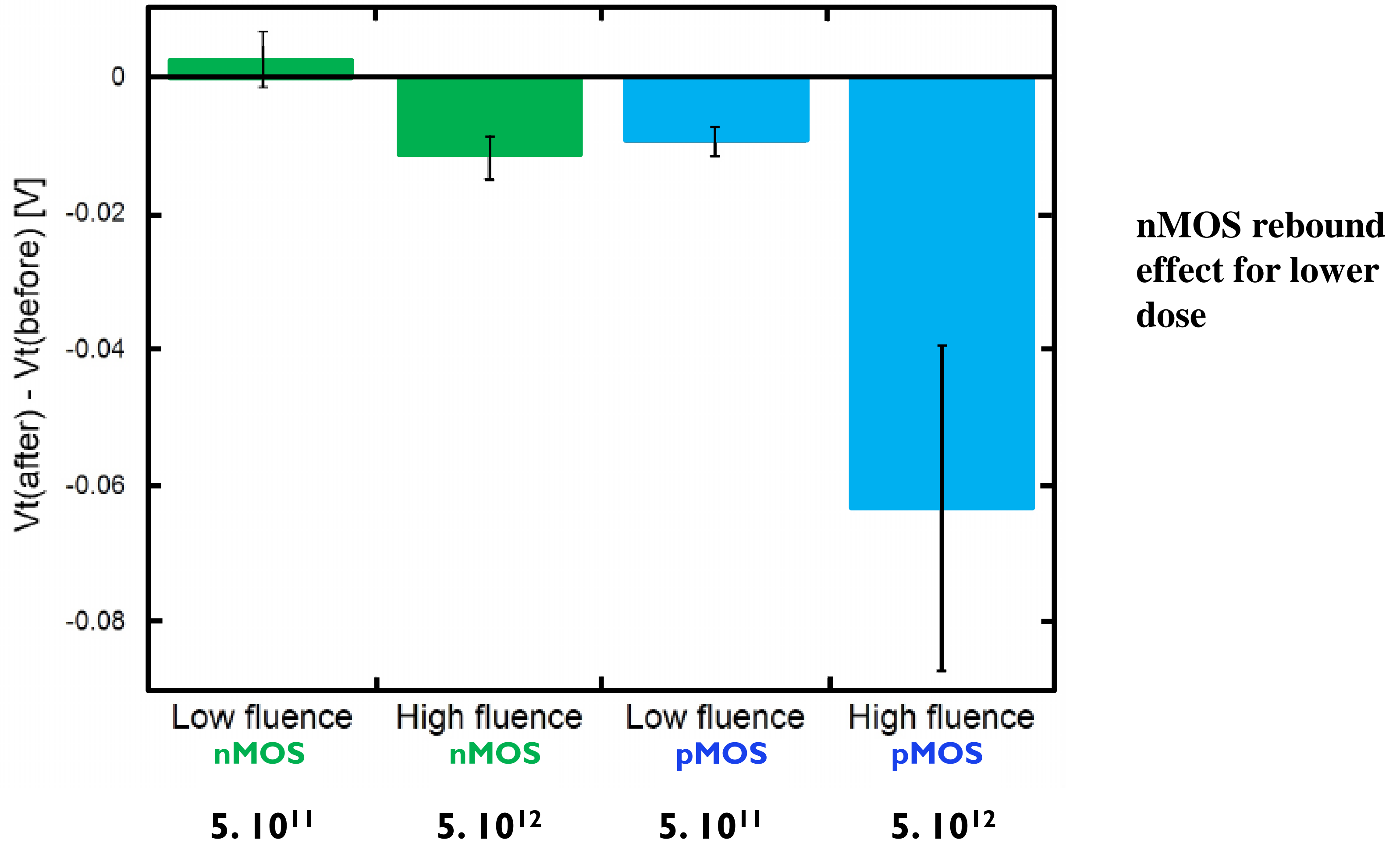




t_{Si} = 15 nm

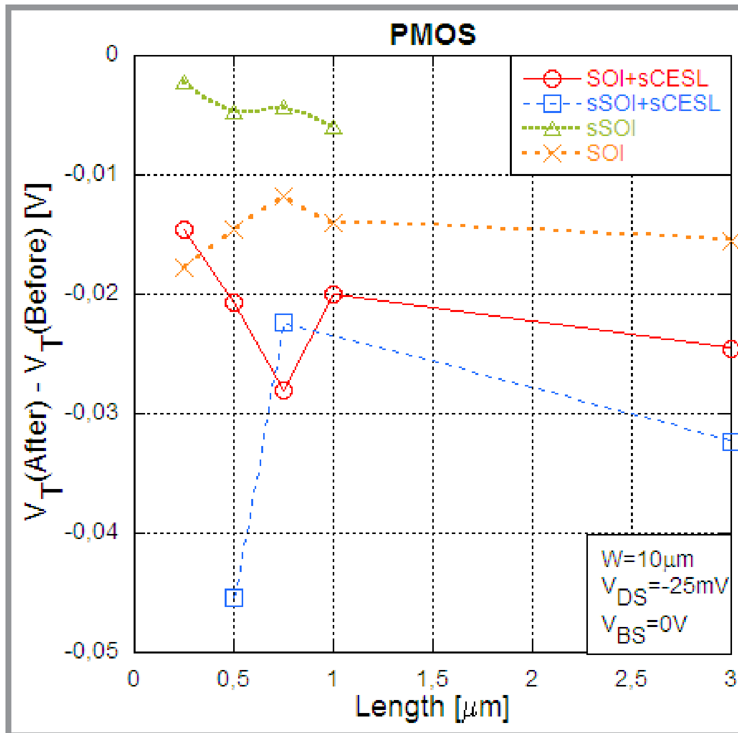
t_{BOX} = 150 nm

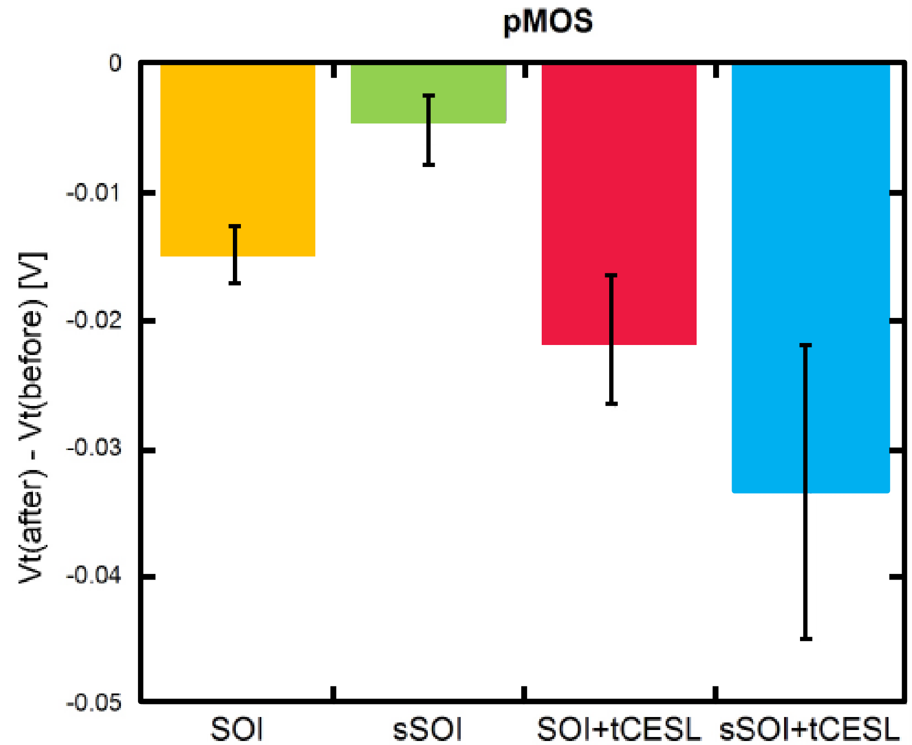
Change in Threshold Voltage for SOI Devices - Dose



nMOS rebound effect for lower dose

Change in Threshold Voltage

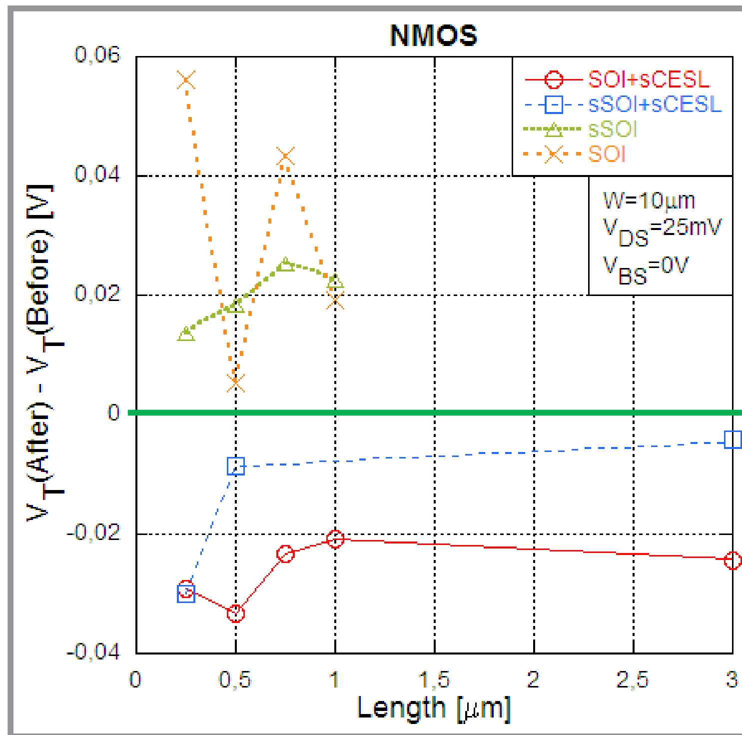


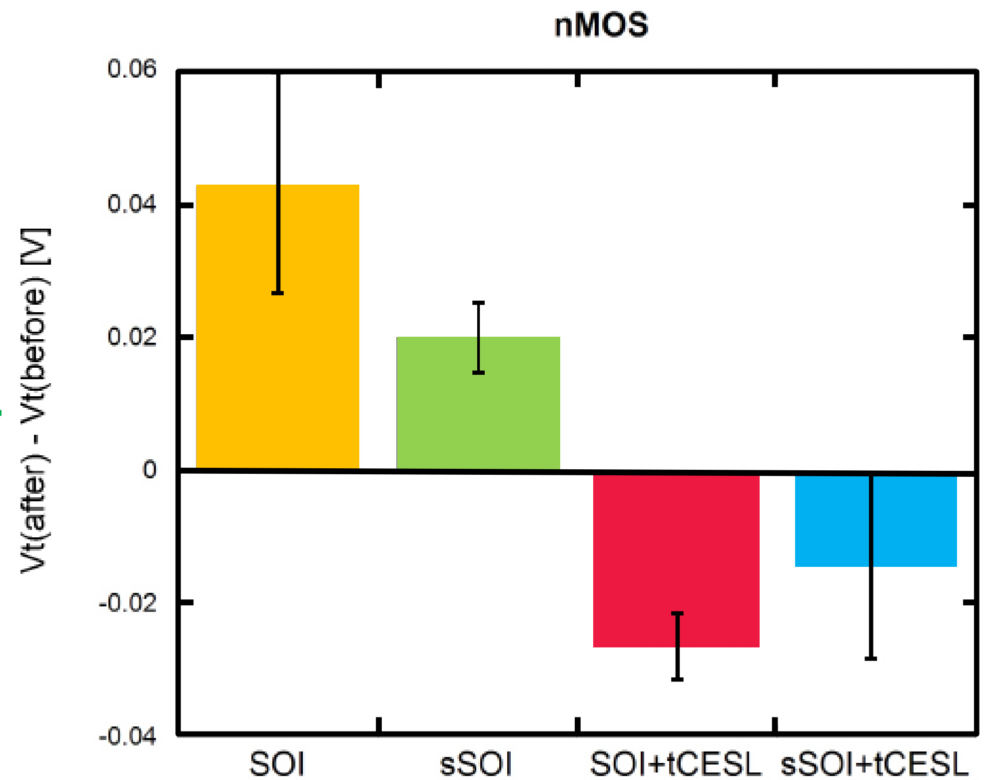


Always ΔV_T negative

More pronounced for sCESL

Change in Threshold Voltage

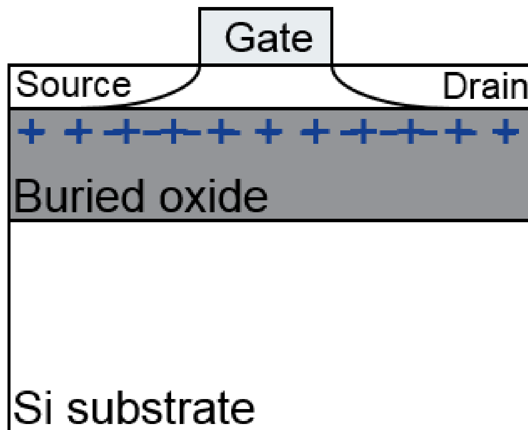


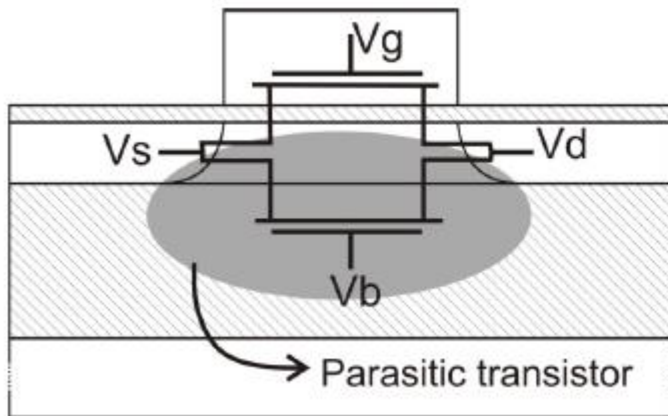


For SOI or sSOI ΔV_T positive

In case of using sCESL DV_T negative

Effect of Radiation on FD SOI Devices





- *PMOS:*
  Radiation creates positive charges in the buried oxide
  - V_T decrease
  - Parasitic transistor turned off

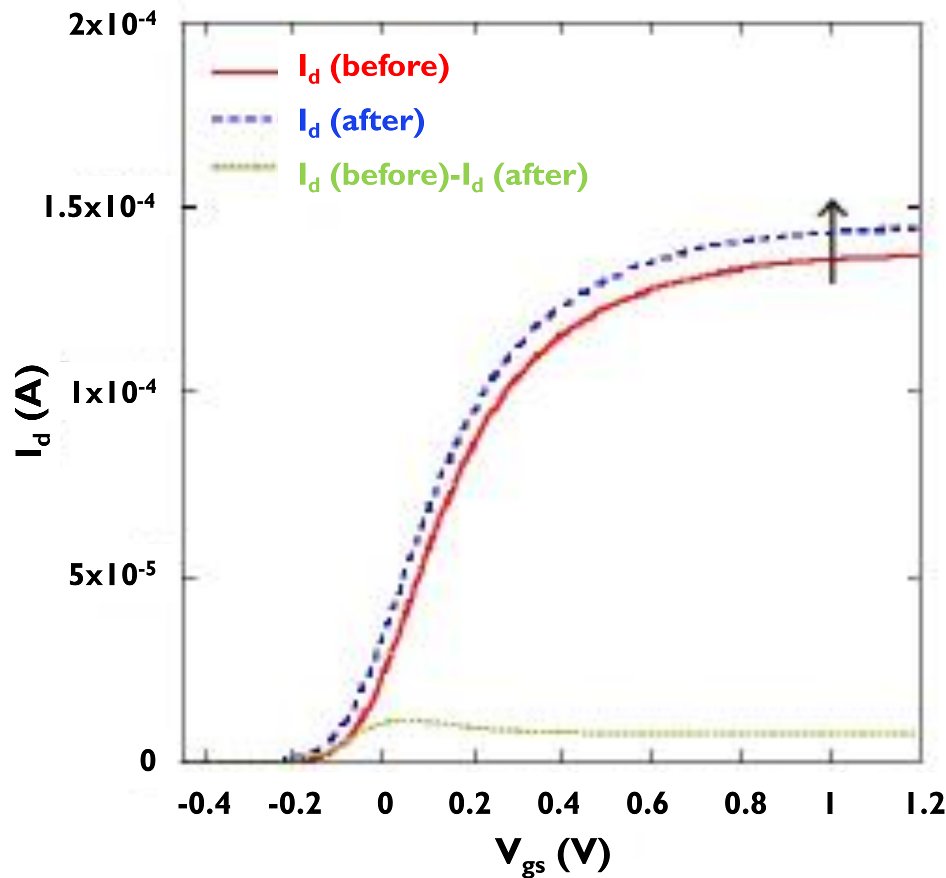
- *NMOS:*
  SOI & sSOI
  Radiation creates negative charges in the buried oxide
  - V_T increase
  - Parasitic transistor turned off

SOI+sCESL & sSOI+sCESL

Radiation creates positive charges in the buried oxide

- V_T decrease
- Parasitic transistor turned on

Fully Depleted SOI Devices



sSOI + tCESL

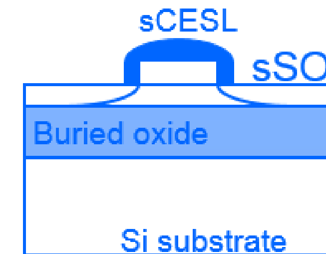
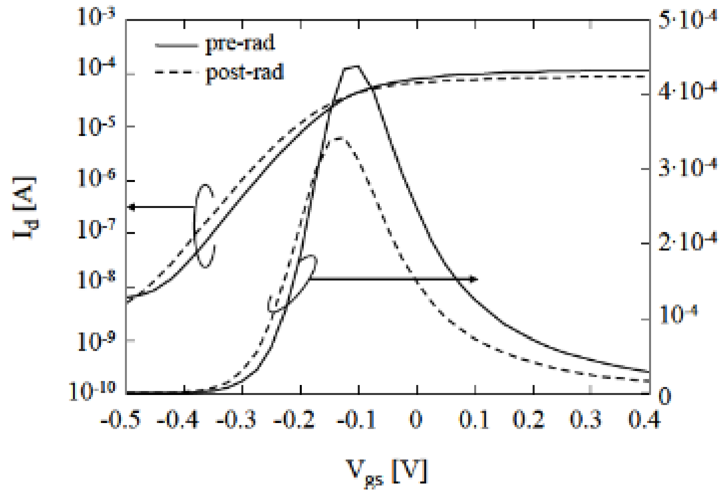
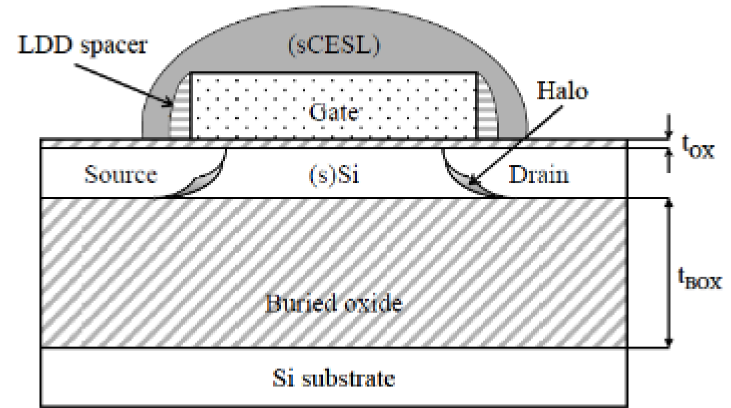
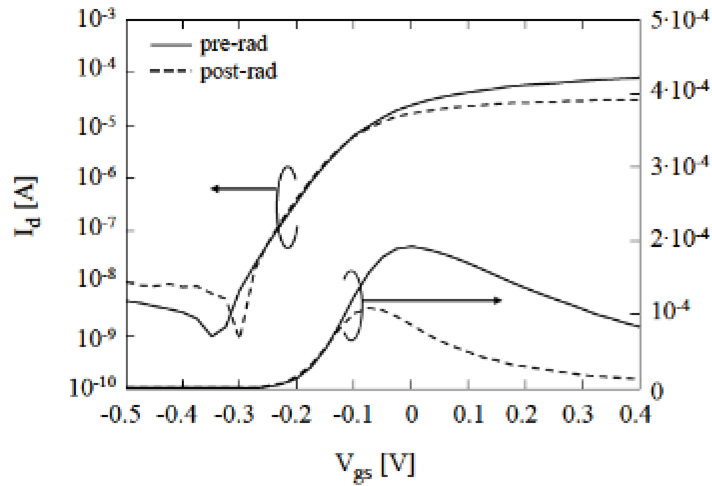


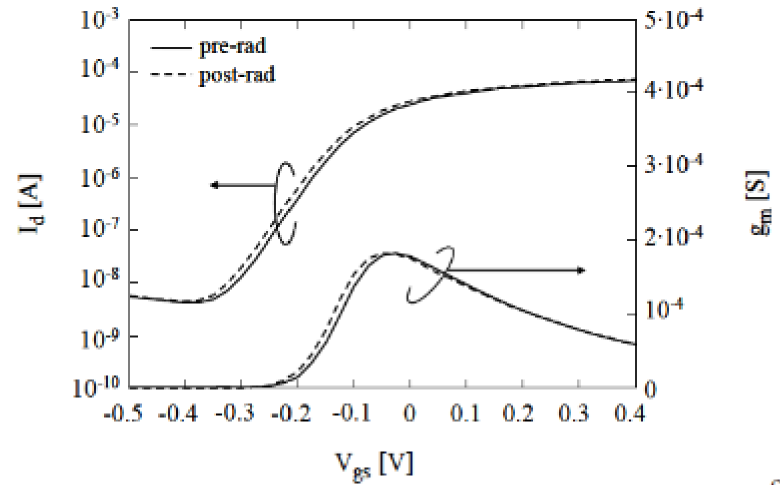
Illustration of the I_d-V_{gs} characteristic before and after 60 MeV, $5x10^{11}$ p/cm^2 proton irradiation and their difference of a SOI+tCESL nMOSFET. W=10 µm, L=0.25 µm, V_B=0 V and V_D=25 mV.

Standard Radiation Behavior FD SOI Devices

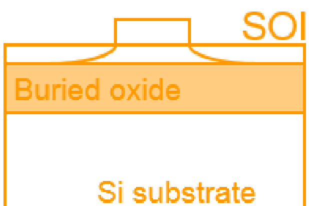


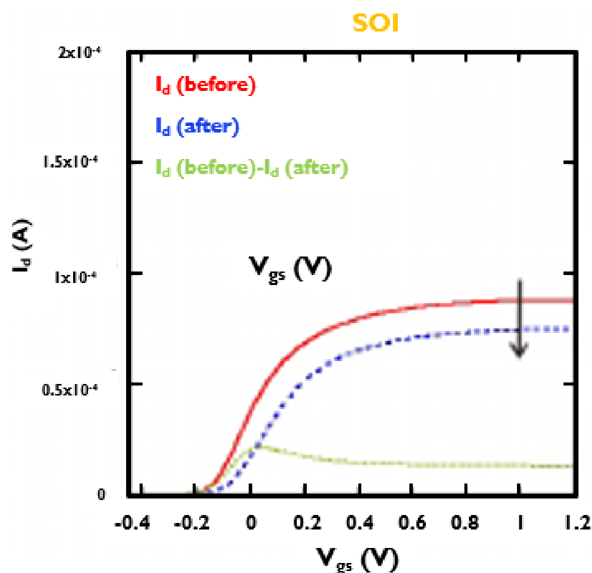


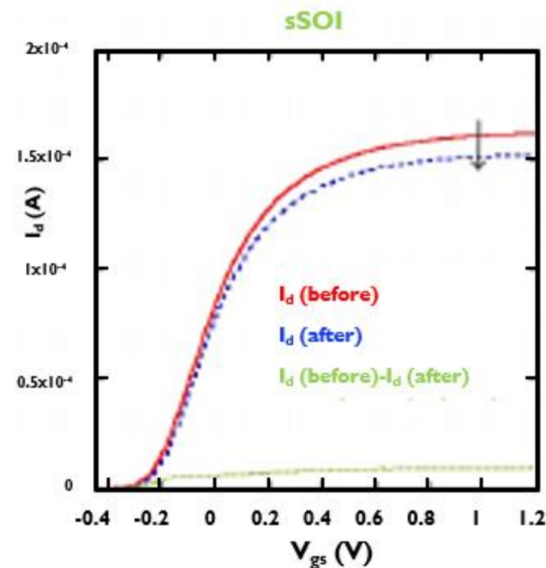


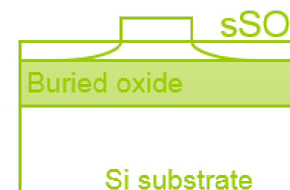


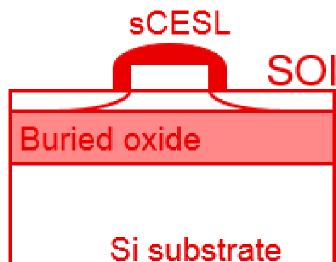
FD nMOS SOI - Strain

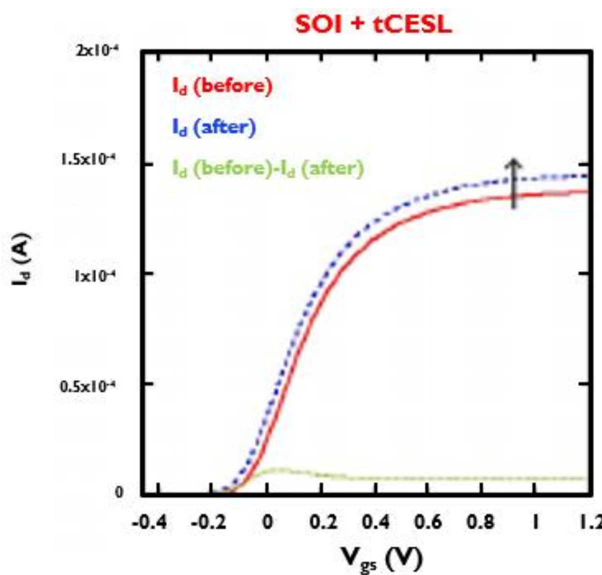


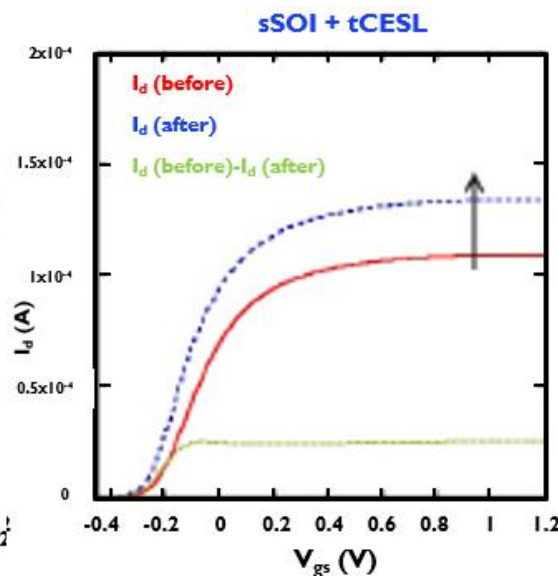


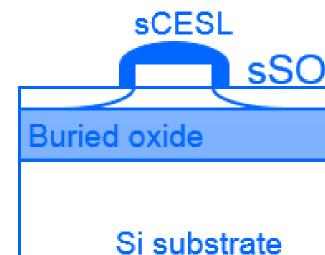












Radiation Behavior sCESL

	NMOS	PMOS
SOI→ SOI+sCESL	Decrease negative charges	Increase positive charges
sSOI→ sSOI+sCESL	Decrease negative charges	Increase positive charges

- The sCESL-layer contains 16 at.% hydrogen
- Due to the proton irradiation, H^+ of the sCESL will migrate towards the buried interface.

Reaction Between H^+ and Dangling Bonds

1. **Depassivation of the already passivated dangling bonds**

$$SiH + H^{+} \rightarrow D^{+} + H_{2}$$

2. **Passivation of the negatively charged dangling bonds**

$$D^{-} + H^{+} \rightarrow SiH$$

3. **No reaction with the positively charged dangling bonds due to Coulomb repulsion**

NMOS (1,2)

Decrease of negative and increase of positive charges

PMOS (1,3)

Increase of positive charges

Radiation Behavior Strained SOI

	NMOS	PMOS
SOI→ sSOI	No effect	Decrease positive charges
SOI+sCESL→ sSOI+sCESL	Increase negative charges	No effect

- **NMOS:** sSi counteracts radiation behavior of sCESL

- **PMOS:** radiation behavior of the combined sSi en sCESL induces more positive charges, in this way the radiation behavior of the strained Si alone will disappear

Stress and Radiation

- **Assessment of effect of sCESL and strained Si on radiation behavior of SOI transistors**

- **Main effect: Creation of charges at the buried oxide/interface**

  - **Interface traps:**
    Negatively charged in NMOSFETs
    Positively charged in PMOSFETs

  - **Trapped hole charge: always positive**

Conclusions Strain

sCESL-layer ➔ high hydrogen concentration

- **NMOS: Passivation of negatively charged interface traps and depassivation already passivated traps**
- **PMOS: only depassivation already passivated trap**

strained Si ➔ influence on radiation effect of sCESL

- **NMOS: Counteract effect of sCESL**
- **PMOS: Enhance effect of sCESL**

nMOS: sSOI+sCESL lowest radiation sensitivity

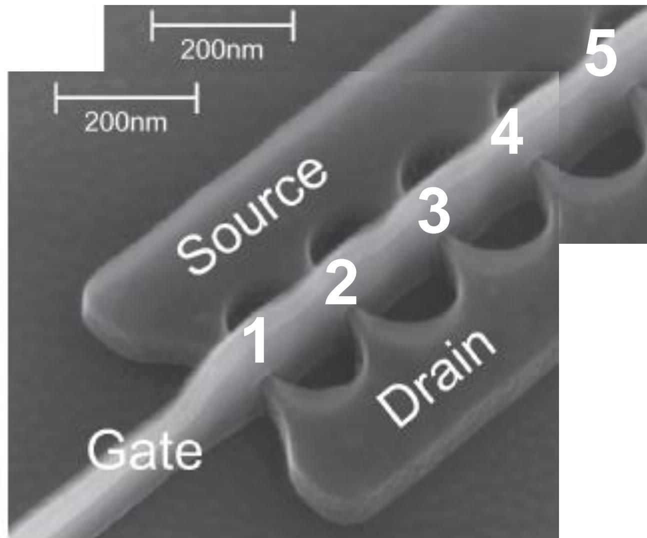
pMOS: sSOI has better radiation behavior compared to SOI

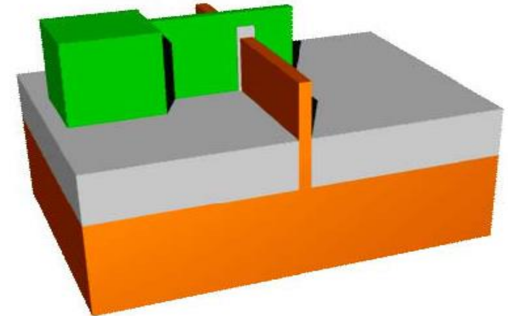
Radiation Hardness SOI and Bulk FinFETs

SOI FinFET

Narrow fin devices
- 5 fins
- W = 25nm
- L = 60nm
- H = 65nm

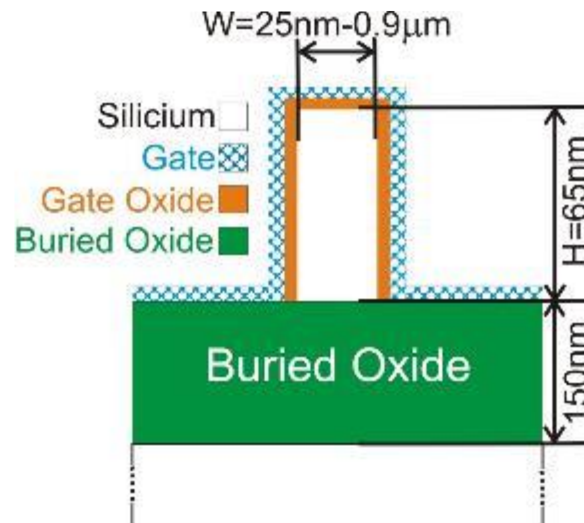
Wide fin devices
- 1 fin
- W = 0.9µm
- L = 0.16µm
- H = 65nm

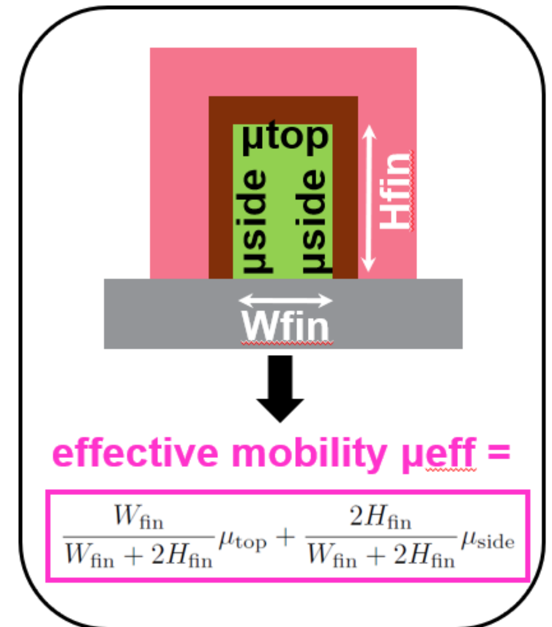




150nm Buried Oxide

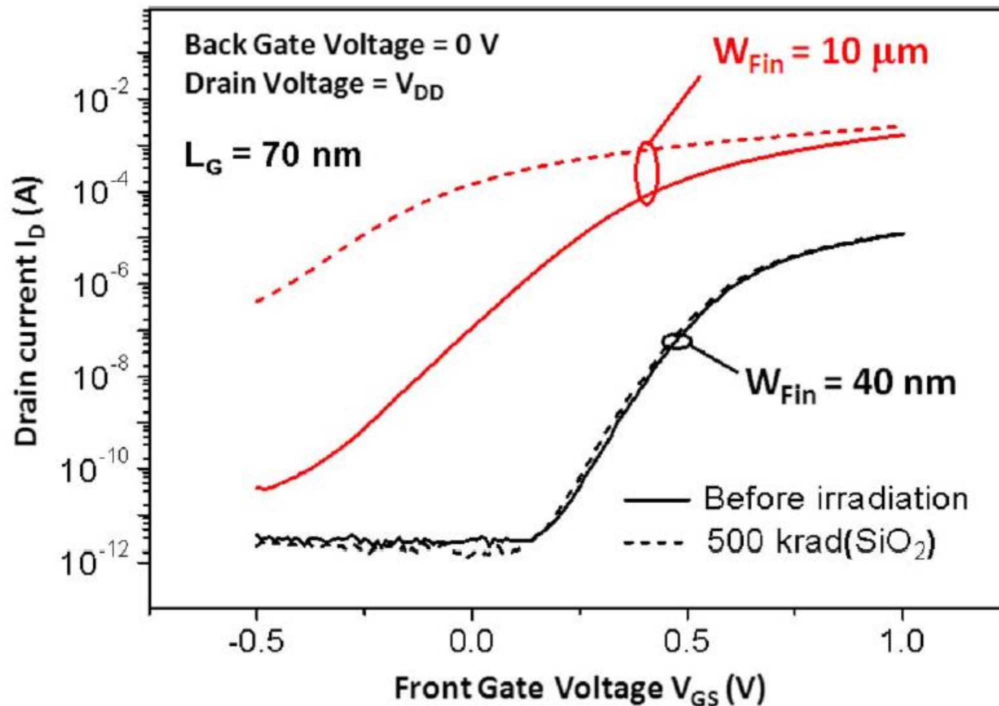
HfSiON gate-dielectric
- 1nm SiO_2 + 2nm HfSiON
- EOT=1.5nm





Radiation FinFET – Impact Fin Width

Radiation tolerance increases with decreasing fin width

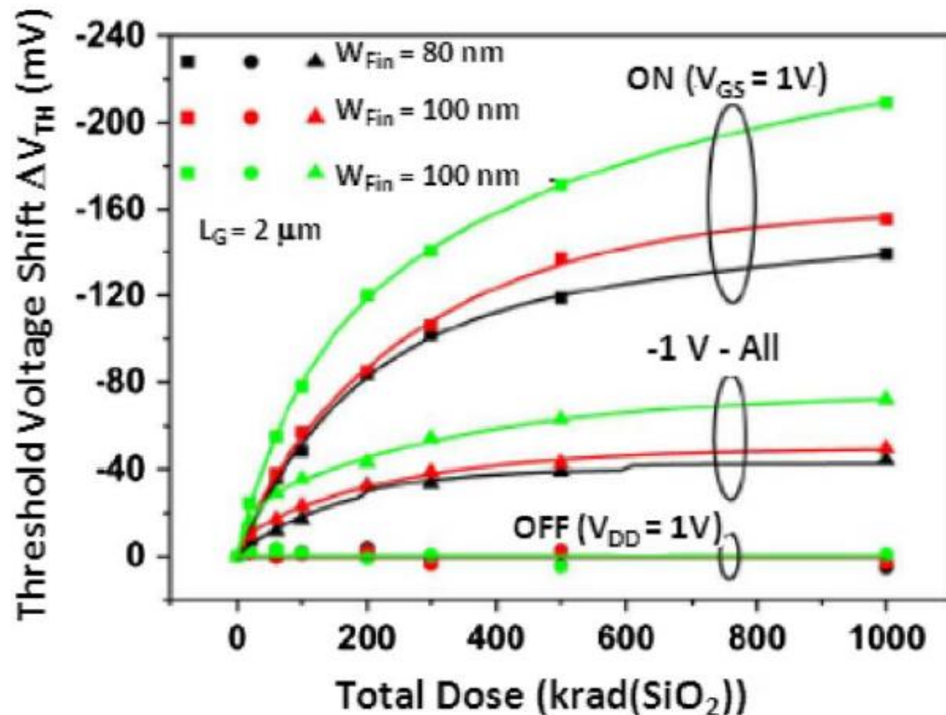


- More efficient control of the lateral gates over the potential in the Si fin for increasing W_{fin}.
- Decreased influence of the BOX, so that the impact of the radiation-induced charges is reduced for larger W_{fin}

Drain current vs gate voltage curve of multiple-gate FETs processed with an Ω-shaped gate with various fin widths, before irradiation and after 500 krad (SiO_2). The drawn gate length is 70 nm . The bias condition during irradiation was the OFF state.

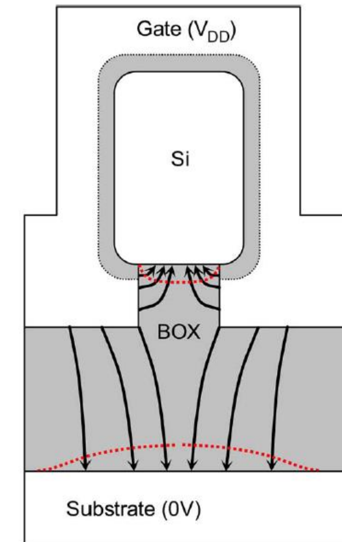
M. Gaillardin, P. Paillet, V. Ferlet-Cavrois, O. Faynot, C. Jahan, and S. Cristoloveanu, "Total ionizing dose effects on triple-gate FETs," IEEE Trans. Nucl. Sci., 53, 3158–3165 (2006)

FinFETs – Bias/Dose Dependence



Threshold voltage shift vs TID measured on triple-gate FETs with different fin width . Different bias conditions during irradiation were applied

- ❑ Bias has a strong impact
- ❑ ON (gate $_{\text{to VDD}}$) is worst condition for TID

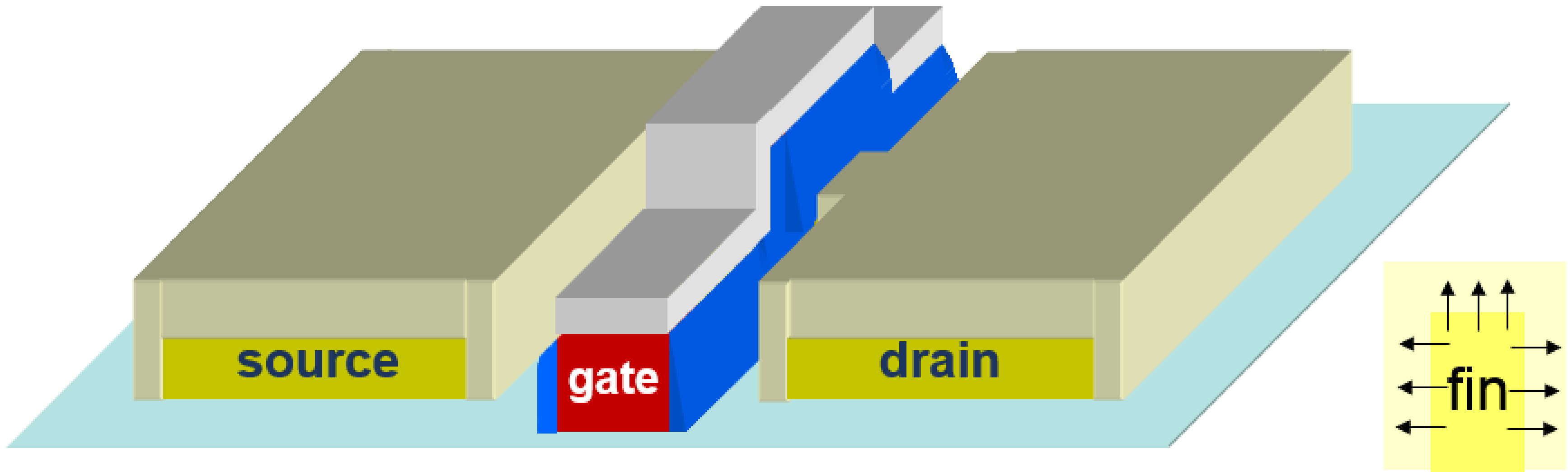


Electric field lines into the BOX for ON-state (gate biased at , other terminals grounded). Red dashed lines correspond to the trapped charge distribution after irradiation (located either at the bottom of the BOX or next to Si Fin)

J.-J. Song, B. K. Choi, E. X. Zhang, R. D. Schrimpf, D. M. Fleetwood, C.-H. Park,Y.-H. Jeong and O.Kim, IEEE Trans. Nucl. Sci., 58, 2871 (2011)

FinFET – Selective Epitaxial Growth

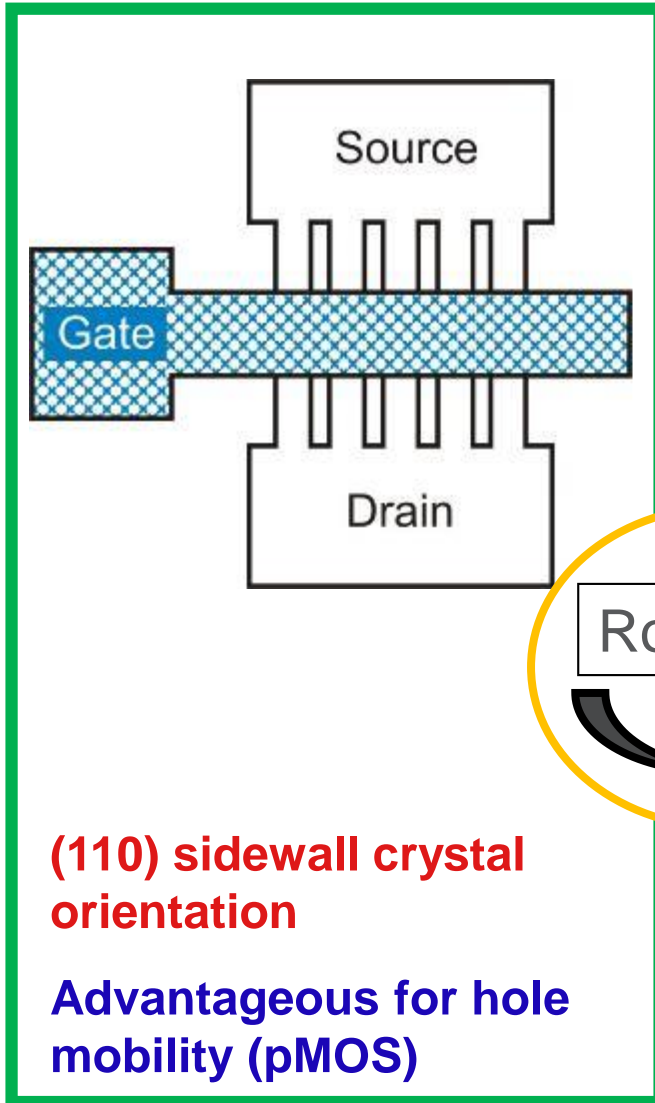
Selective epitaxial growth on the S/D areas (SEG)

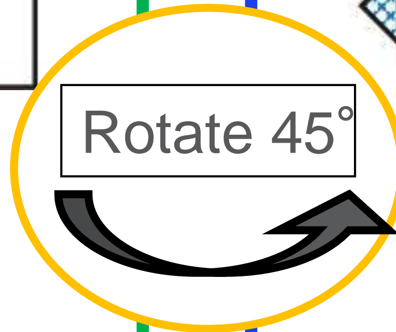


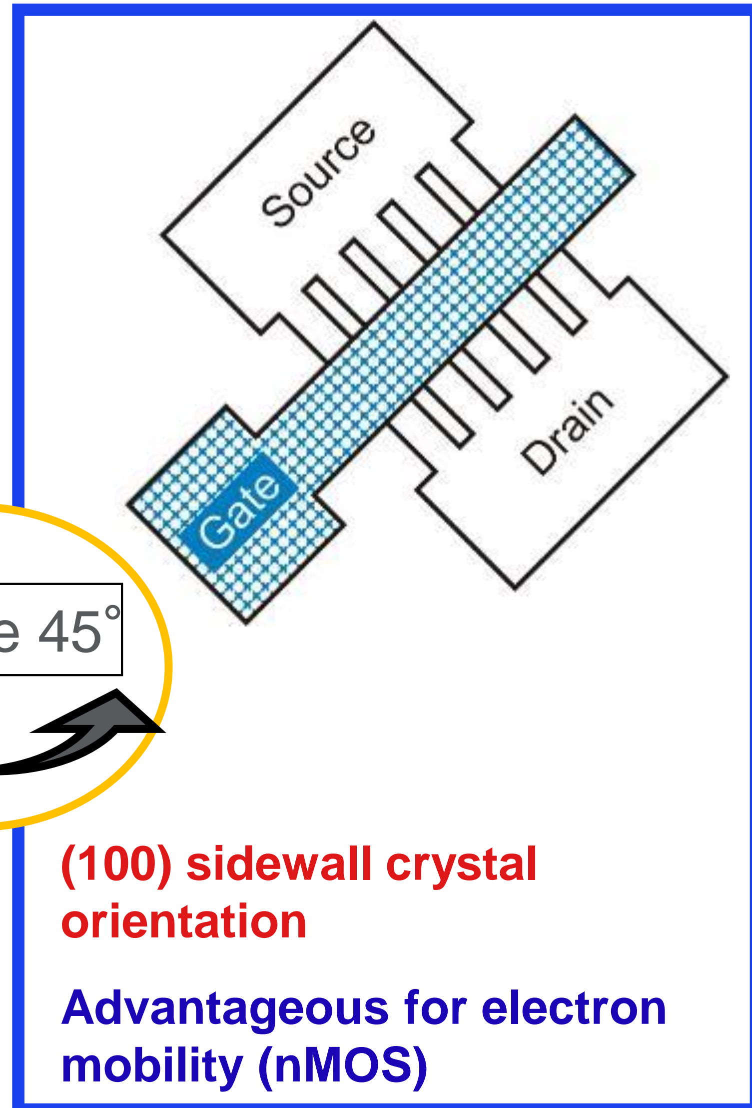
Narrow fins introduce a large S/D resistance

SEG needed to increase thickness in all directions and decrease R_{CON}

FinFET – 45° Rotation







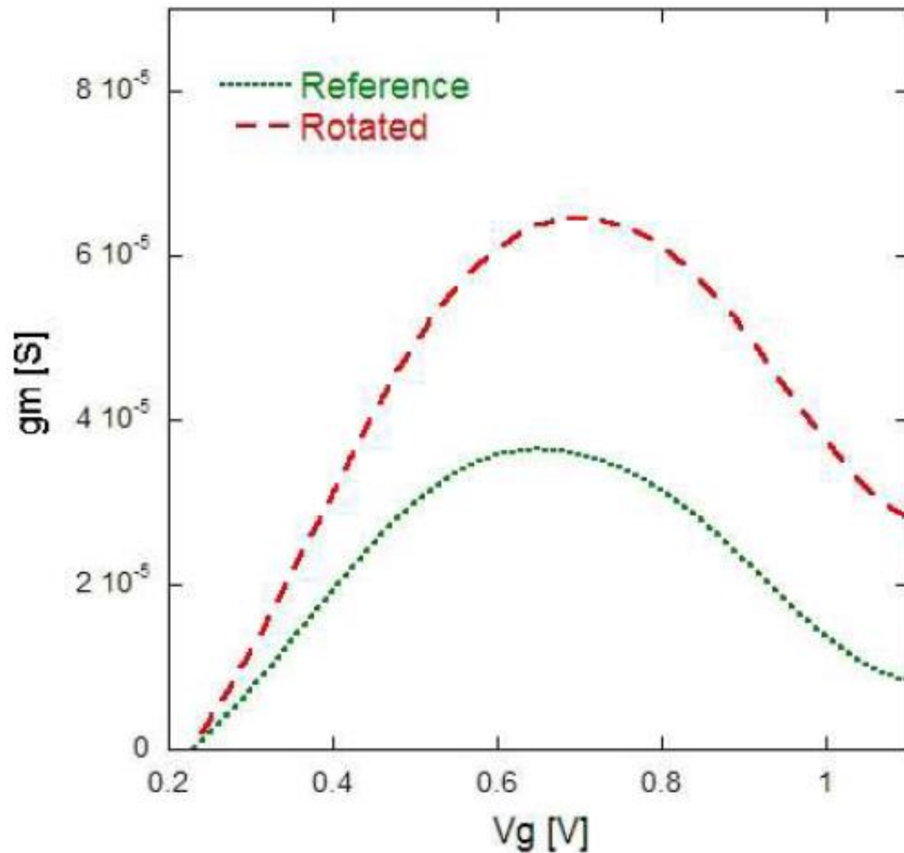
(110) sidewall crystal orientation

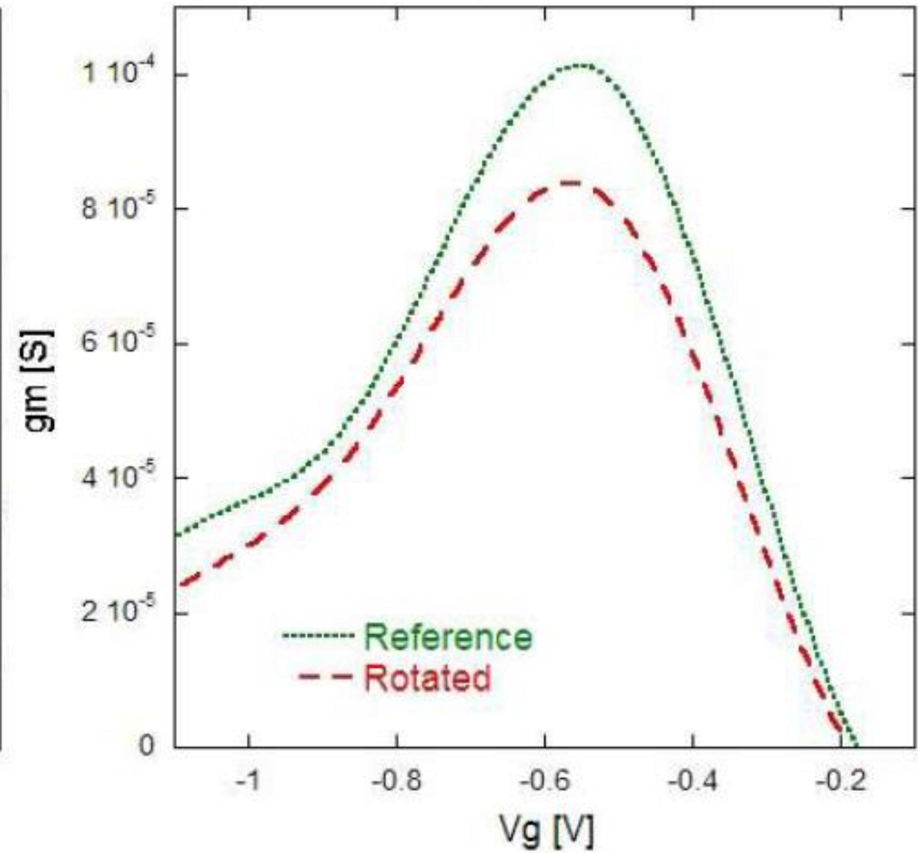
Advantageous for hole mobility (pMOS)

(100) sidewall crystal orientation

Advantageous for electron mobility (nMOS)

Transconductance FinFET – 45° Rotation



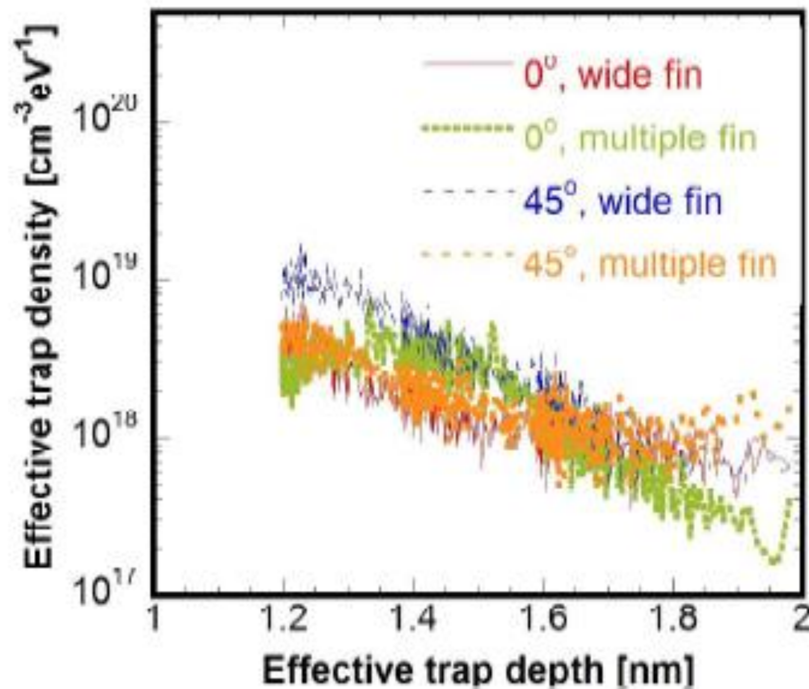


Transconductance as function of V_{GS}, for n- and pFinFETs for standard orientation (reference) and 45 ° rotation of the fins. W_{fin} = 25 nm, L = 60 nm, IV_{ds}I = 50 mV.

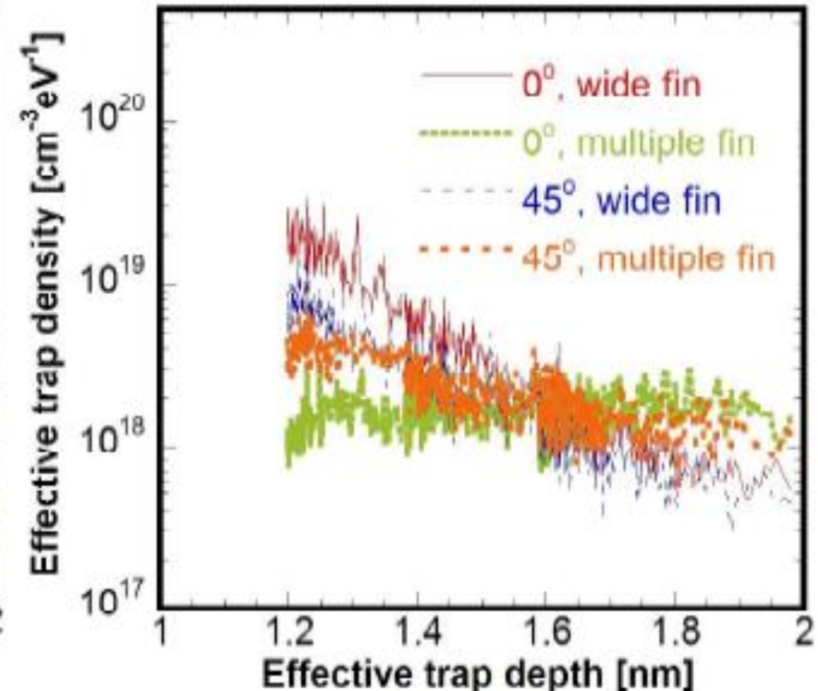
SOI FinFET – 45° Rotation

No specific impact of the orientation

nFinFET

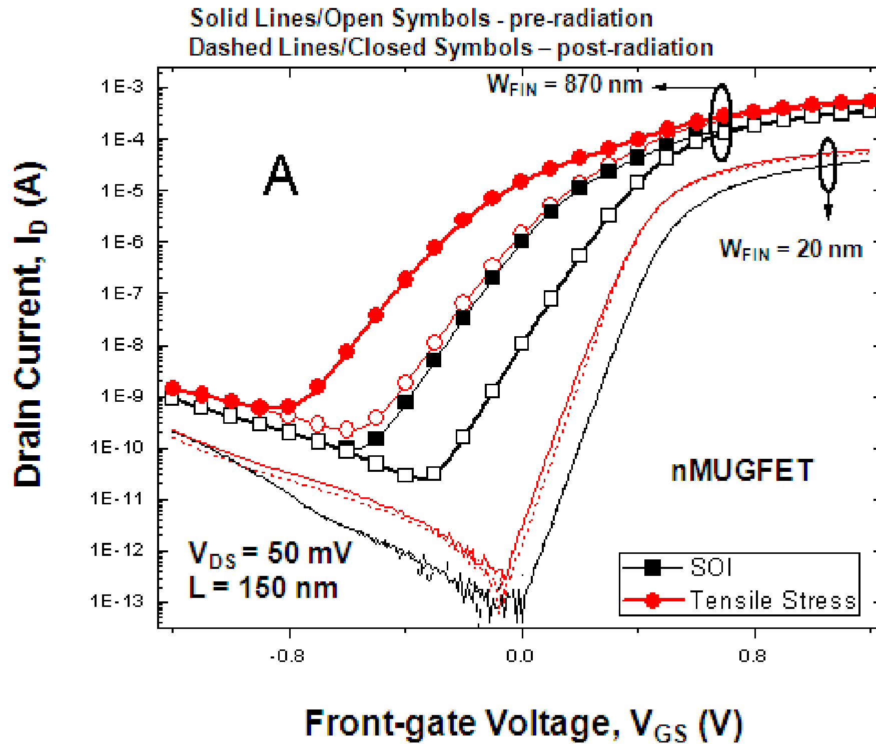


pFinFET



Comparison of the effective trap density versus effective trap depth for standard orientation (reference) and 45 ° rotation of the fins. Both a single wide fin (W_{fin} = 1 µm) and 5 fins (W_{eff} = 0.75 µm). No SEG and HfSiON gate. L = 0.15 µm, IV_{ds}I = 50 mV.

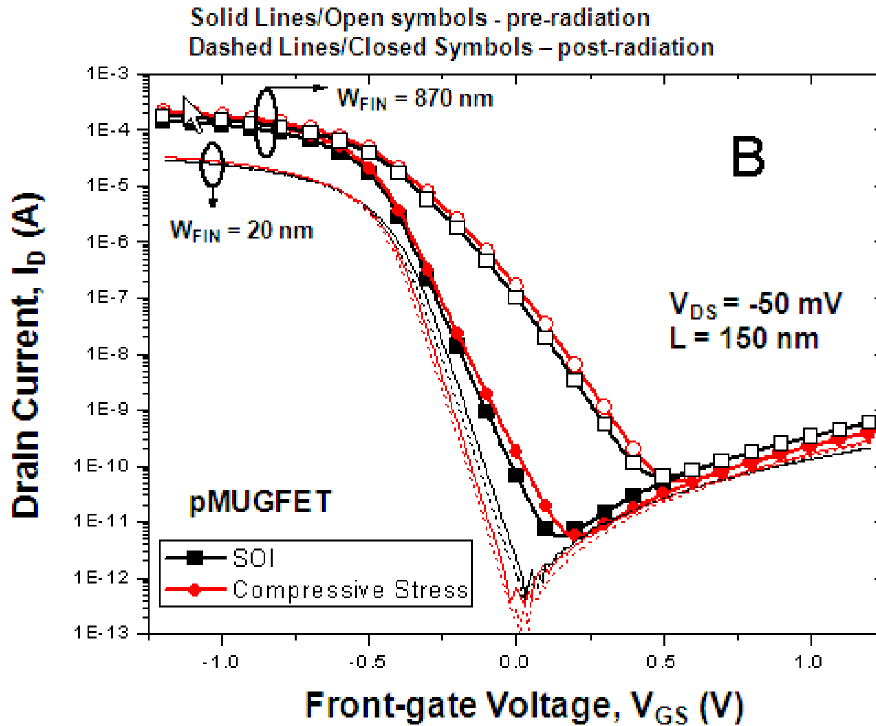
Drain Characteristics Proton Radiations - nMuGFET



I_D as a function of V_{GS}, for nMuGFETs, before and after radiation (60 MeV protons) for two different device widths. Tensile stress are used.

- Tensile stress improve the performance
- Smaller width device have a better radiation hardness

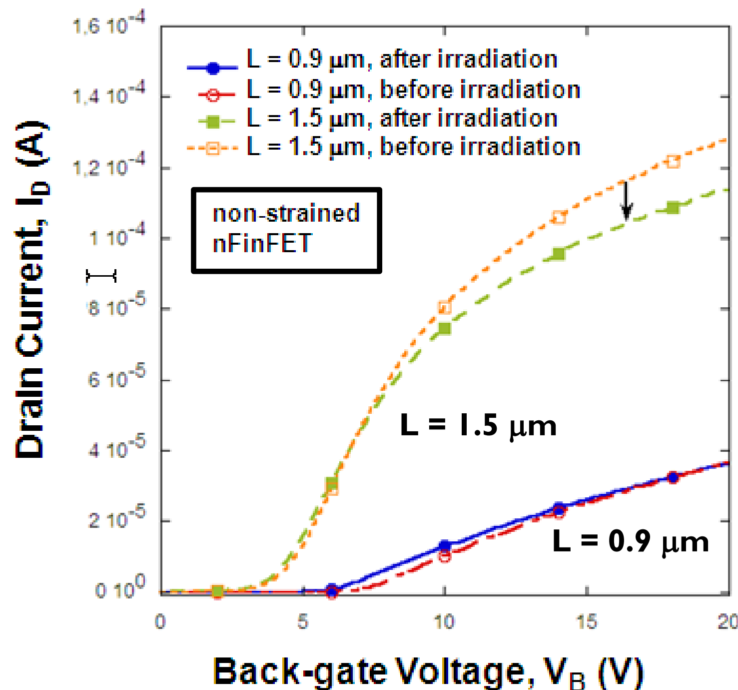
Drain Characteristics Proton Radiations - pMuGFET

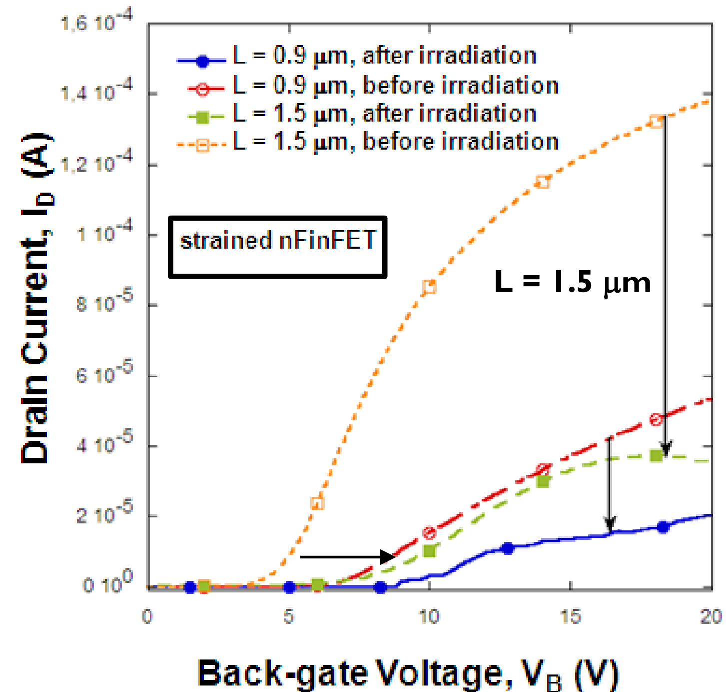


I_D as a function of V_{GS}, for pMuGFETs, before and after radiation (60 MeV protons) for two different device widths. Compressive stress are used.

- **Impact compressive stress is limited**
- **Smaller width device have a better radiation hardness**

Impact Radiation Back-channel Transistor





Degradation of the back-channel transistor due to an 10^{12} cm^{-2} proton irradiation for non-strained and strained (1.5 GPa tensile) nFinFETs with two different gate lengths.

Strained back-channel transistor

- More are more degraded than unstrained
- Degradation = mobility degradation due to interface traps
- V_T more positive after irradiation (negative charge in nMOS)

Impact Radiation Back-channel Transistor

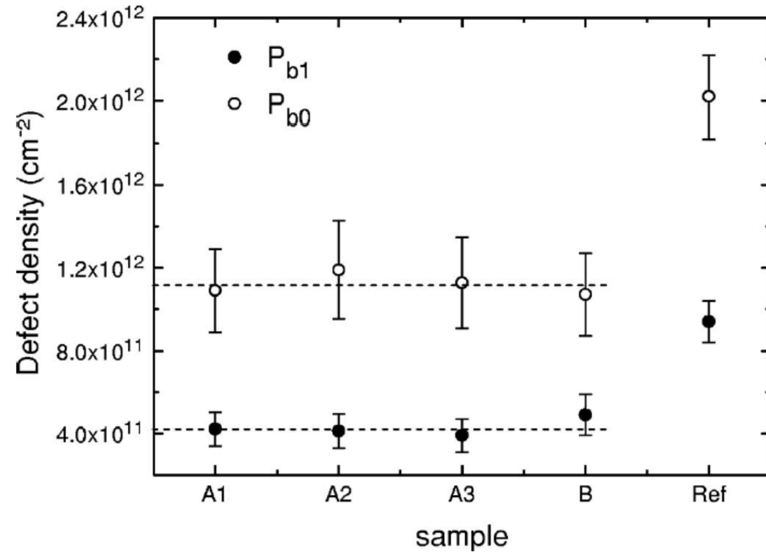
Degradation = mobility degradation due to interface traps (negative charge in nMOS)

		L=0.15 μm	L=0.9 μm
Before irradiation [$cm^2/V \cdot s$]	Non-strained	620	570
	Strained	720	740
After irradiation [$cm^2/V \cdot s$]	Non-strained	570	500
	Strained	310	290
Relative difference [%]	Non-strained	8	13
	Strained	57	61

Mobility degradation of the back-channel transistor before and after 60 MeV 10^{12} p/cm^2. W_{fin} = 9 mm, Vds = 25 mV and V_{gs} = 0 V.

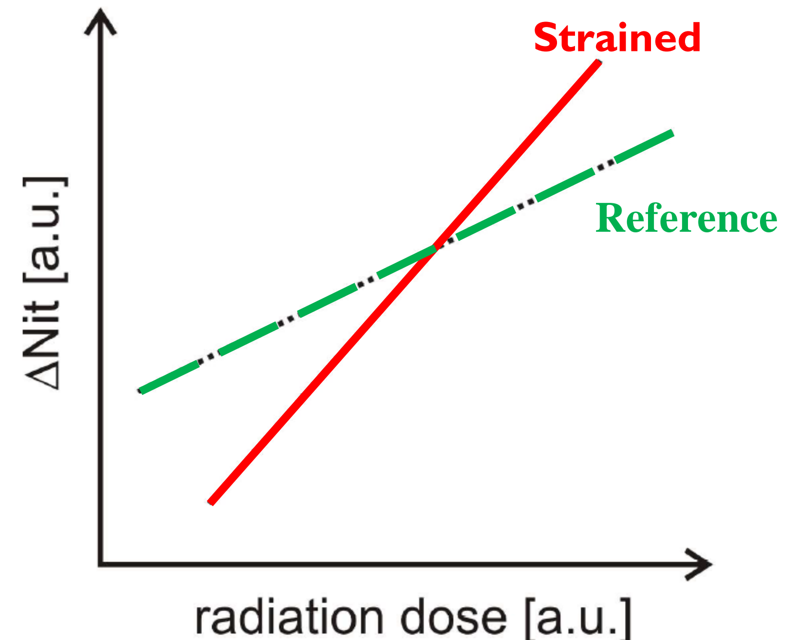
Impact of Strain in Function of Radiation Level

Stress leads to a lower level of dangling bonds

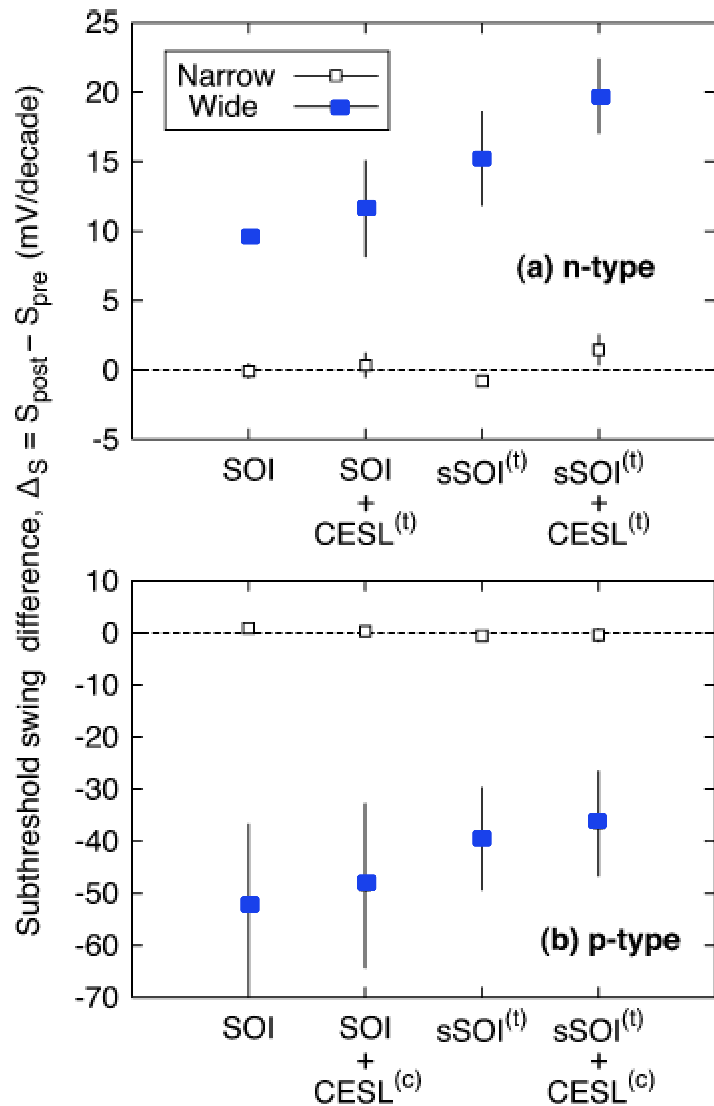


P. Somer, A. Stesmans, V.V. Afanas'ev, C. Claeys and E. Simoen, JAP 103 (2008) 033703

Low dose irradiations may result in less radiation-induced charges for strained devices due to the lower dangling bonds concentration



Radiation – Subthreshold Swing



$$\Delta\mu = \mu_{post}/\mu_{pre}$$

$$\Delta\mu = \frac{1}{1 + a\Delta Nit}$$

$$\Delta\mu = \frac{1}{1 + b\Delta SS}$$

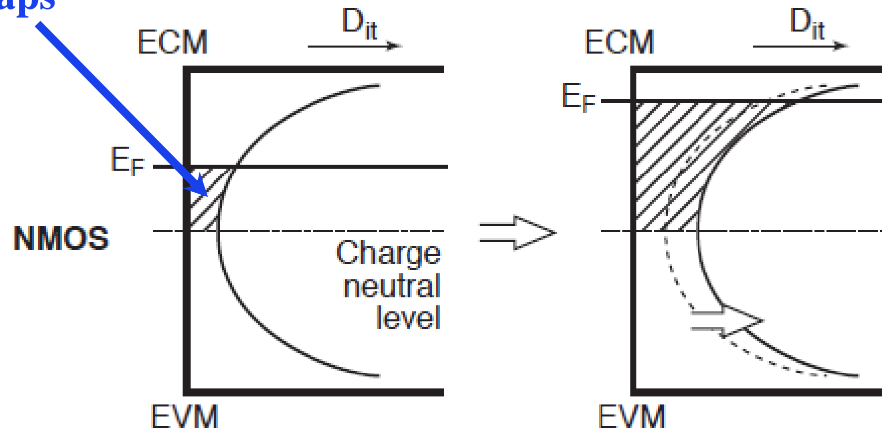
Proton: 60 MeV, 10^{12} p/cm^2

D. Kobayashi, E. Simoen, S. Put, A. Griffoni, M. Poizat, K. Hirose and C. Claeys, IEEE TNS, 58, 800 (2011)

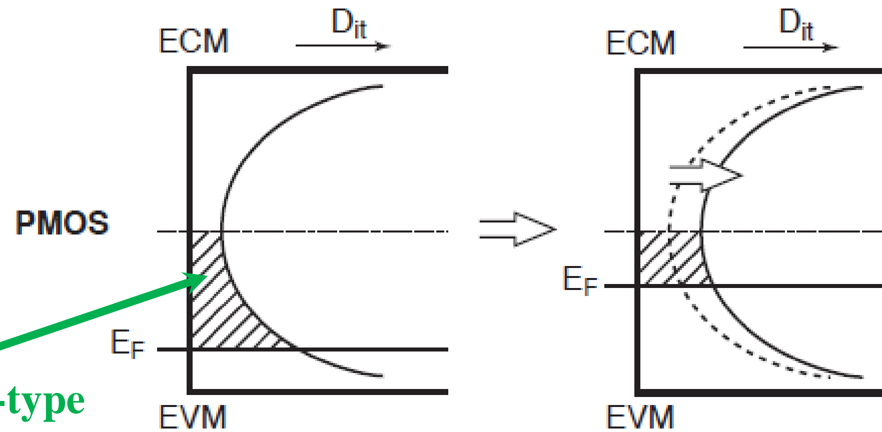
Radiation – Subthreshold Swing

ΔSS comes from charge in the Si/BOX interface due to charged interface traps by radiation

Acceptor-type traps



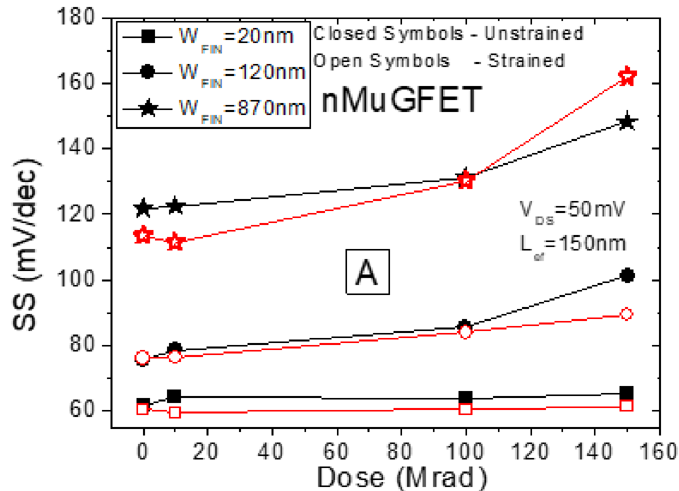
n(↑) more acceptor-type traps

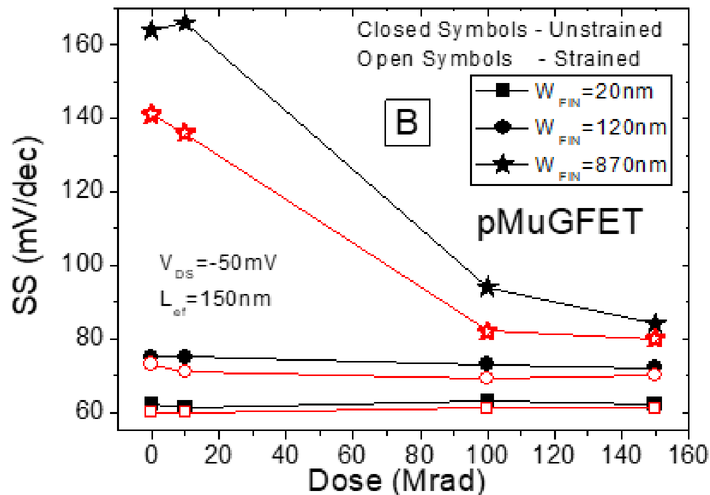


Donor-type traps

p(↓) less donor-type traps

X-Ray Radiation – Subthreshold Swing MuGFETs



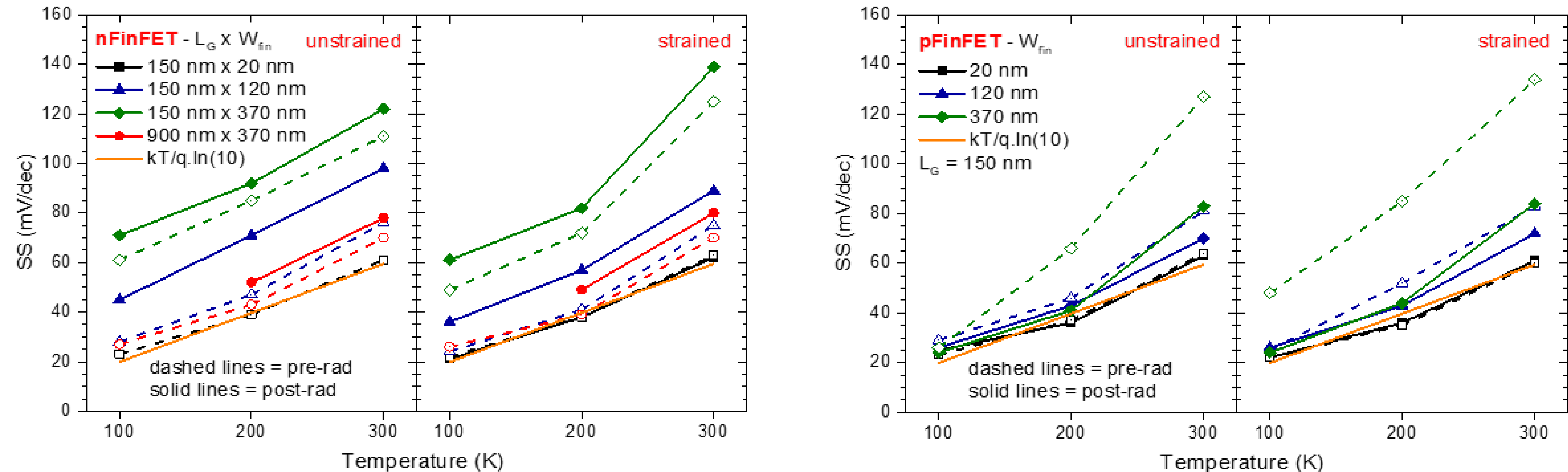


- SS is lower for strained devices
- SS increases for wider devices
  - Poorer control coupling between sidewall gates and channel
- X-ray radiation has less impact for smaller devices
  - V_T shift and interface charges
- For nMuGFETs SS increases after radiation:
  - Increased charges increase the off-state leakage current
- For pMuGFETs the off-state current is suppressed
  - More pronounced for wider devices

C.C.M. Bordallo, F.F. Teixeira, M.G. Silveira, J.A. Martino, P.G.D. Agopian, E. Simoen and C. Claeys, Semecond Sci. Techn., 29, 125015 (2014)

Proton Radiation – Subthreshold Swing vs Temperature

60 MeV, 10^{12} p/cm^2



- Radiation impacts both N_{it} and therefore SS
- Strain gives a higher N_{it}
- For p-channel devices reduces back-channel conduction (radiation-induced charges)
- Low temperature reduces the V_T and impacts the back-channel conduction

L.F.V. Caparroz, C.C.M. Bordallo, J.A. Martino, E. Simoen, C. Claeys and P.G.D. Agopian, Proc. EUROSOI-ULIS 2017

SOI P-MuGFETs Neutron Radiation

Processing

- 200 mm SOI and sSOI (1.5 GPa biaxial strain)
- Si film = 65 nm, BOX = 150 nm
- Gate stack: 2 nm HfSiON on 1 nm SiO_2 (EOT = 1.5 nm) + 5 nm TiN covered by 100 nm poly-Si
- SEG at 750°C for S/D

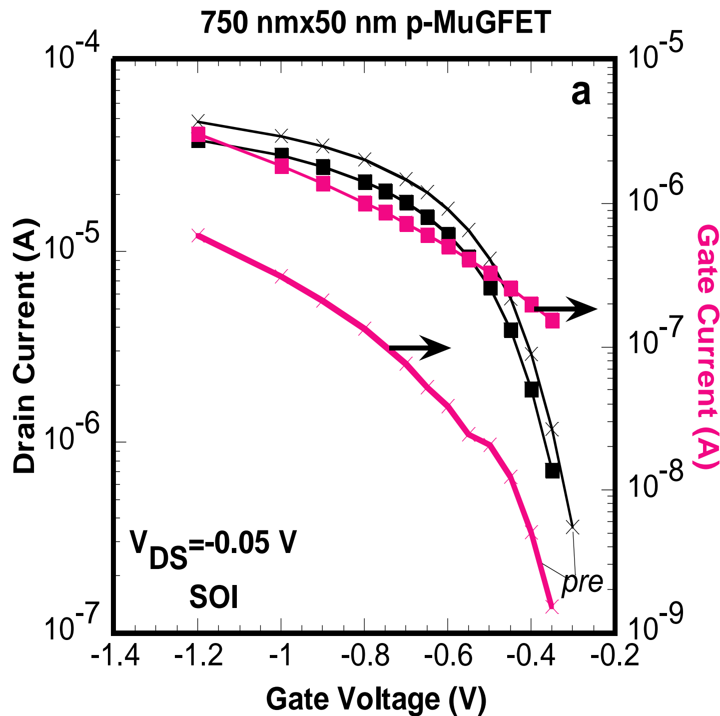
Radiation

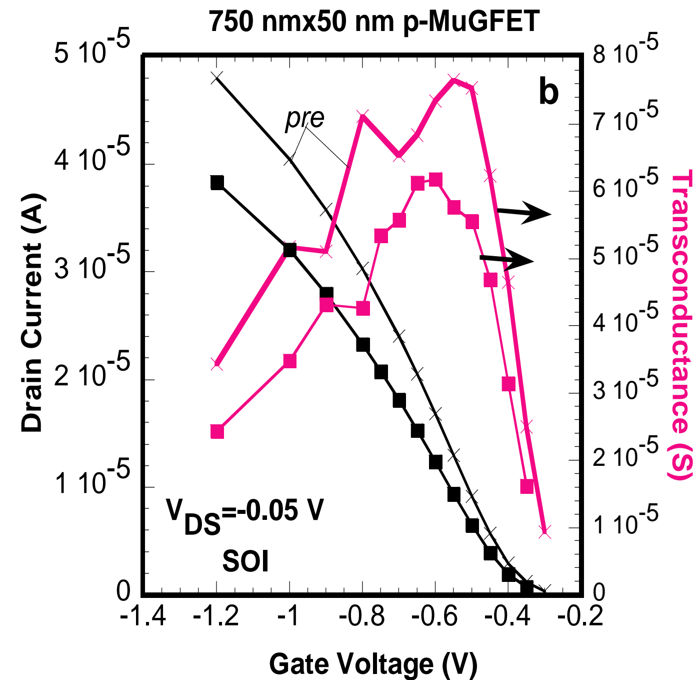
Neutron irradiation at LLN (CYCLONE), Belgium

- Energy spectra 5 to 45 MeV (peak 20 MeV)
- Fluence: 1.8 x 10^{14} n/cm^2 (1-2% area deviation)
- Concomitant γ-rays about 2.4%
- Contacts floating

D. Kobayashi, E. Simoen, S. Put, A. Griffoni, M. Poizat, K. Hirose and C. Claeys, IEEE TNS, 58, 800 (2011)

Gate Current, Drain current, Transconductance – Neutron Irradiations

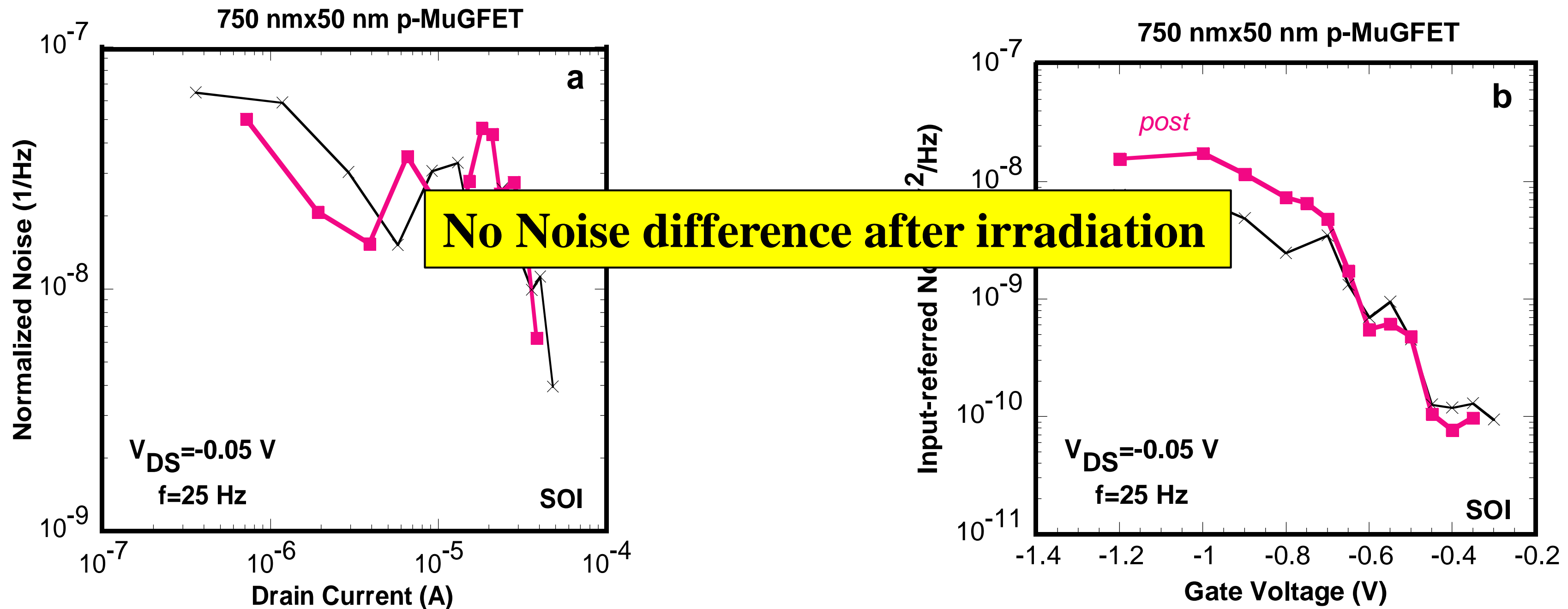




Gate and drain current in linear operation versus front gate voltage V_{GS} (a) and I_D and g_m versus V_{GS} (b) for a 750 nmx50 nm SOI p-MuGFET in linear operation. The pre-rad (x) curves are compared with the post neutron-irradiation (■) characteristics.

E. Simoen, S. Put, N. Collaert, C. Claeys, V. Kilchytska, J. Alvarado and D. Flandre, Proc. SBMicro (2010)

Normalized Drain Current Noise/Input-referred Noise PSD – Neutron Irradiations



Normalized drain current noise spectral density versus drain current (a) and input-referred noise spectral density S_{VG} (b) at a frequency f=25 Hz for a 50 nm SOI p-MuGFET before (x) and after (■) neutron irradiation.

E. Simoen, S. Put, N. Collaert, C. Claeys, V. Kilchytska, J. Alvarado and D. Flandre, Proc. SBMicro (2010)

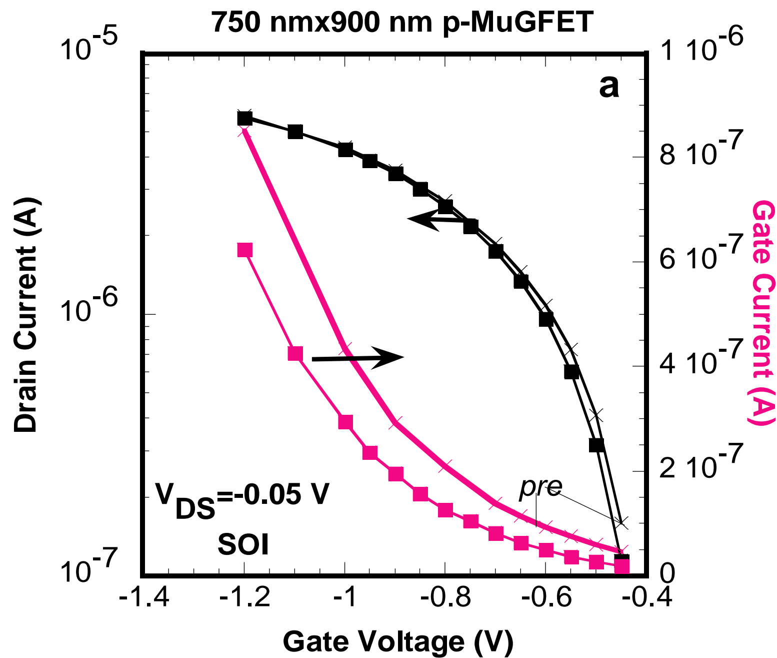
Normalized Drain Current Noise/Input-referred Noise PSD – Neutron Irradiations

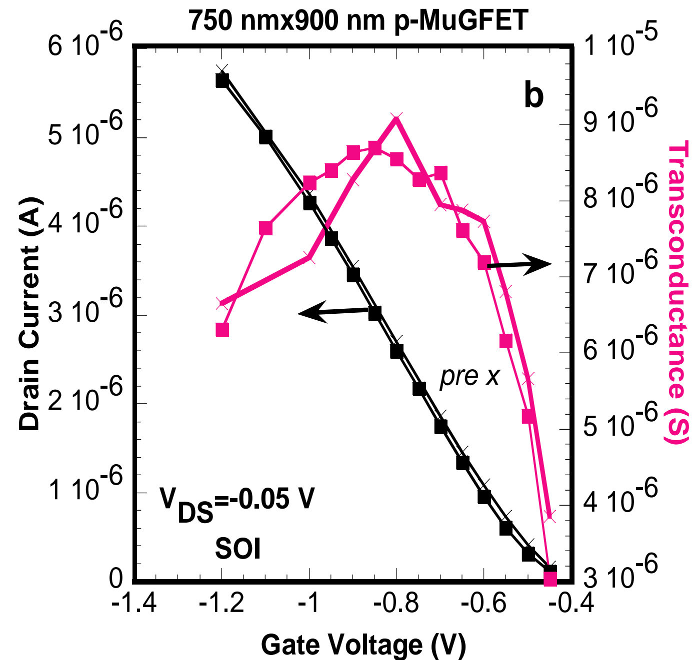
- **No impact of radiation on LF noise performance**
- **LF noise caused by number fluctuation (McWhorter) related to oxide traps within 1-2 nm from the Si/SiO_2 interface**
- **Increased S_{VG} for negative V_{GS}**

→ **increase in series resistance ?**
increase in gate current?

E. Simoen, S. Put, N. Collaert, C. Claeys, V. Kilchytska, J. Alvarado and D. Flandre, Proc. SBMicro (2010)

Gate Current, Drain current, Transconductance – Neutron Irradiations (Case 2)

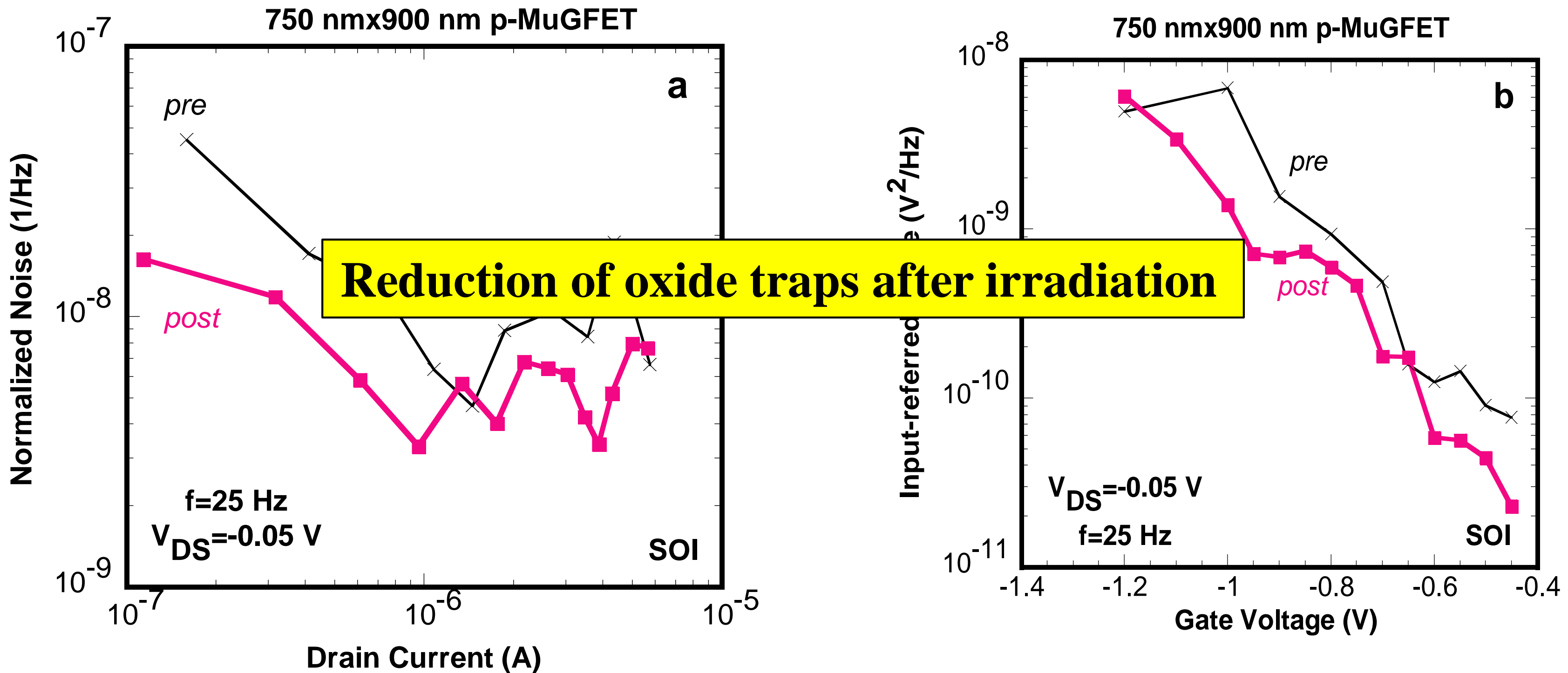




Gate and drain current in linear operation versus front gate voltage V_{GS} (a) and I_D and g_m versus V_{GS} in function of V_{GS} (b) for a 750 nmx900 nm SOI p-MuGFET in linear operation. The pre-rad (x) curves are compared with the post neutron-irradiation (■) characteristics.

E. Simoen, S. Put, N. Collaert, C. Claeys, V. Kilchytska, J. Alvarado and D. Flandre, Proc. SBMicro (2010)

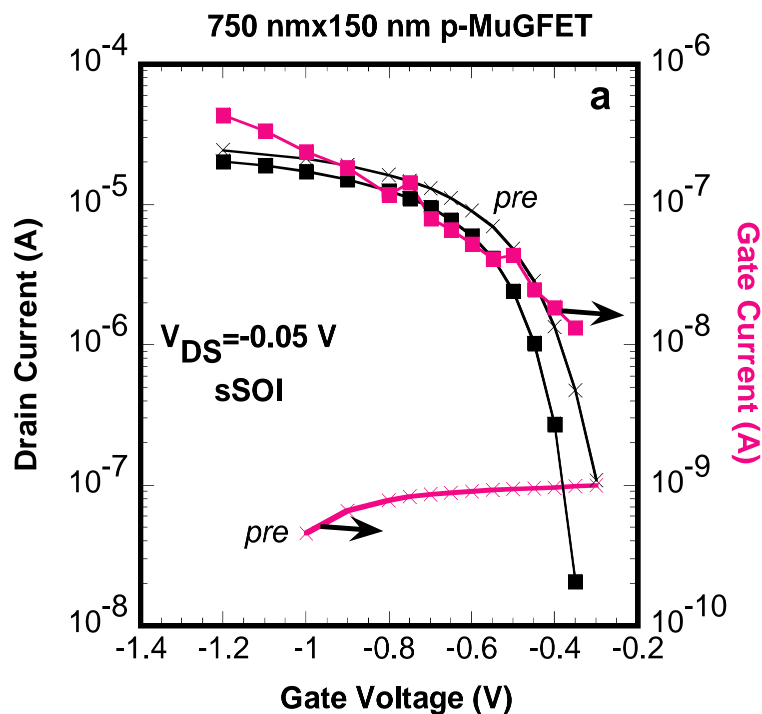
Normalized Drain Current Noise/Input-referred Noise PSD – Neutron Irradiations (Case 2)

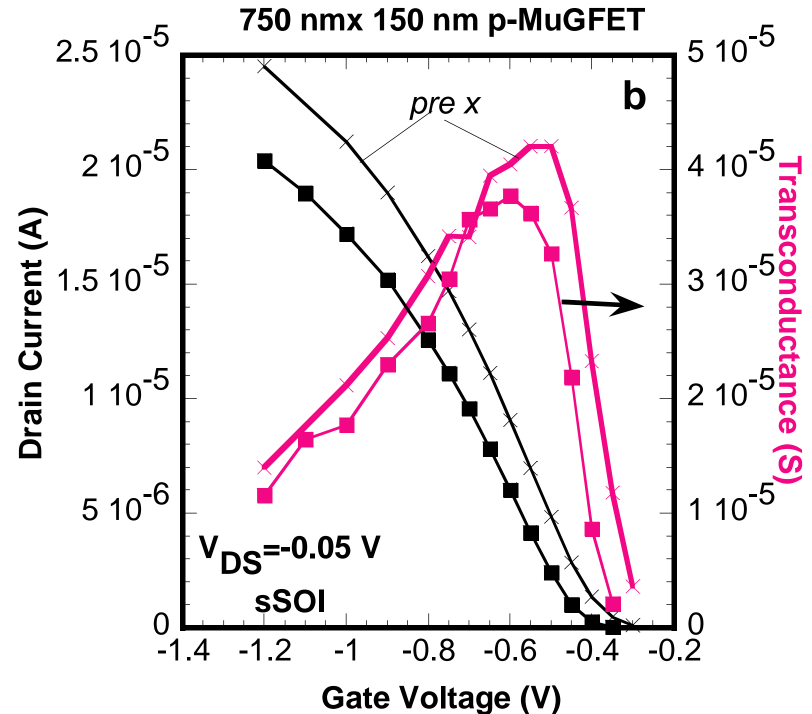


Normalized drain current noise spectral density versus drain current (a) and input-referred noise spectral density S_{VG} (b) at a frequency f=25 Hz for a 900 nm SOI p-MuGFET before (x) and after (■) high-energy neutron irradiation.

E. Simoen, S. Put, N. Collaert, C. Claeys, V. Kilchytska, J. Alvarado and D. Flandre, Proc. SBMicro (2010)

Gate Current, Drain current, Transconductance – Neutron Irradiations (Case 3)

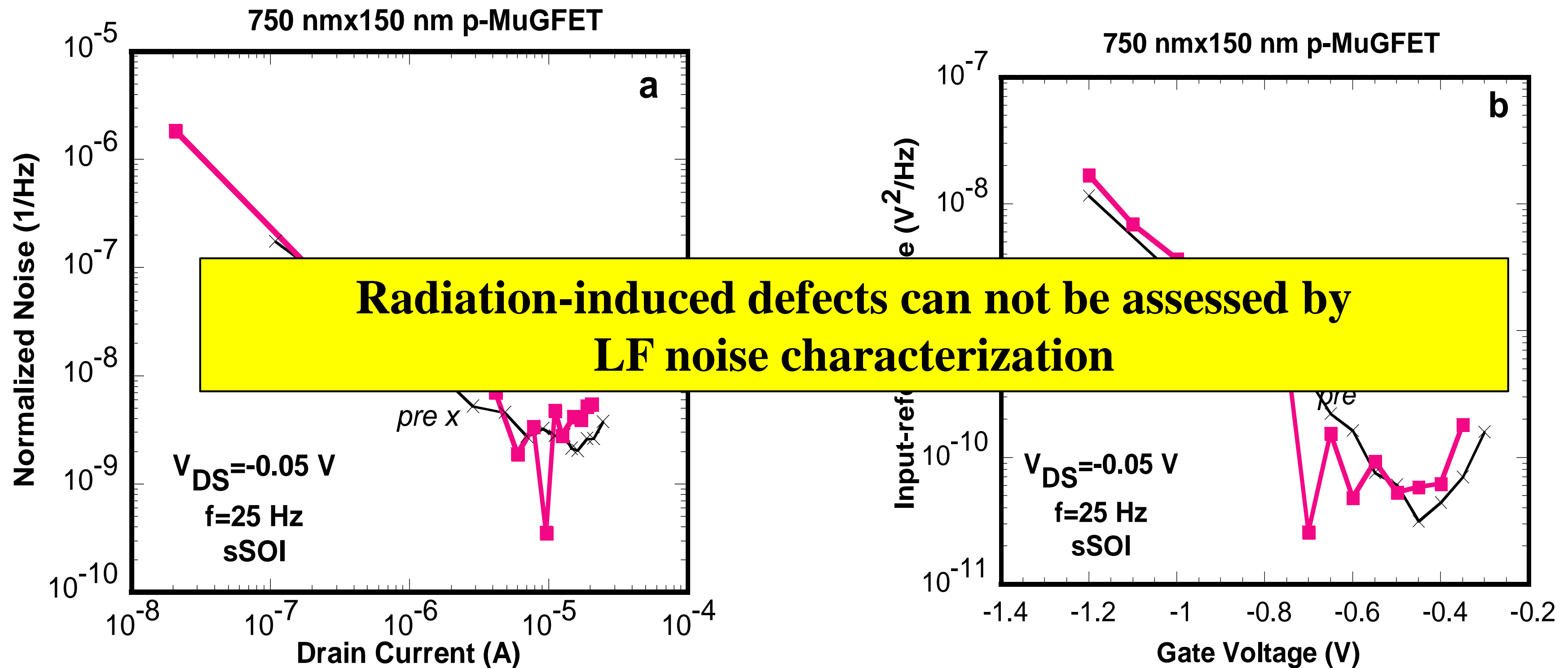




Gate and drain current in linear operation versus front gate voltage V_{GS} (a) and I_D and g_m versus V_{GS} in function of V_{GS} (b) for a 750 nmx150 nm sSOI SOI p-MuGFET in linear operation. The pre-rad (x) curves are compared with the post neutron-irradiation (■) characteristics.

E. Simoen, S. Put, N. Collaert, C. Claeys, V. Kilchytska, J. Alvarado and D. Flandre, Proc. SBMicro (2010)

Normalized Drain Current Noise/Input-referred Noise PSD – Neutron Irradiations (Case 3)



Normalized drain current noise spectral density versus drain current (a) and input-referred noise spectral density S_{VG} (b) at a frequency f=25 Hz for a 150 nm sSOI p-MuGFET before (x) and after (■) high-energy neutron irradiation.

E. Simoen, S. Put, N. Collaert, C. Claeys, V. Kilchytska, J. Alvarado and D. Flandre, Proc. SBMicro (2010)

Conclusion SOI p-FinFETs Neutron Irradiations

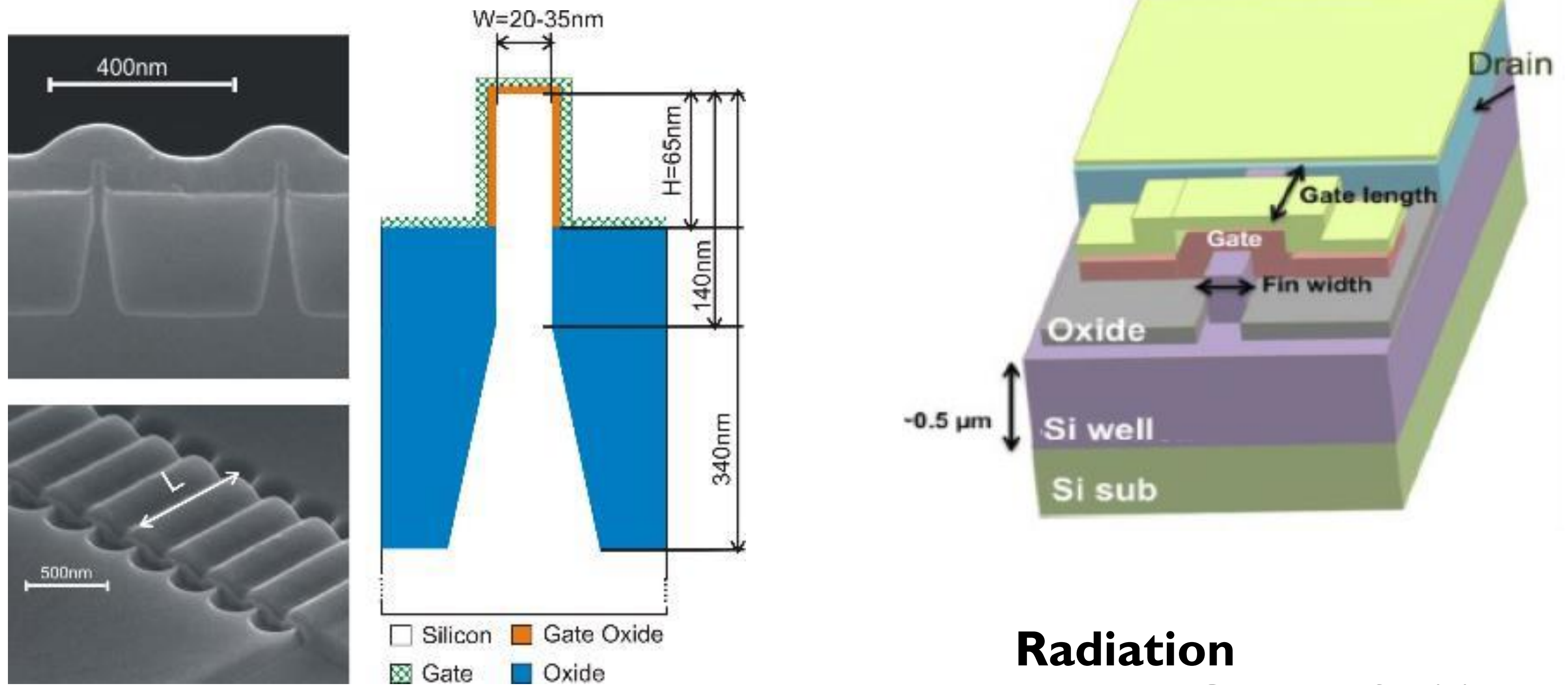
There is statistical distribution of the post-irradiation performance

- Some devices have a catastrophic degradation
- Smaller part of the devices is hardly affected
- Some devices even have a lower gate leakage current and reduced LF noise behavior
- Noise can be caused by defects in the nitride spacer or the sidewall oxide

Re-ordering or curing effect

- There is no impact of the strain observed

Bulk FinFETs



Radiation

BRIGITTE-facility

10kGy (1kGy/h)

T=328K

Floating contacts

300 mm Cz Si, L = 65 nm, W = 20-35 nm

Dielectric: 1 nm SiO_2 + 2.6 nm 40% HfSiON

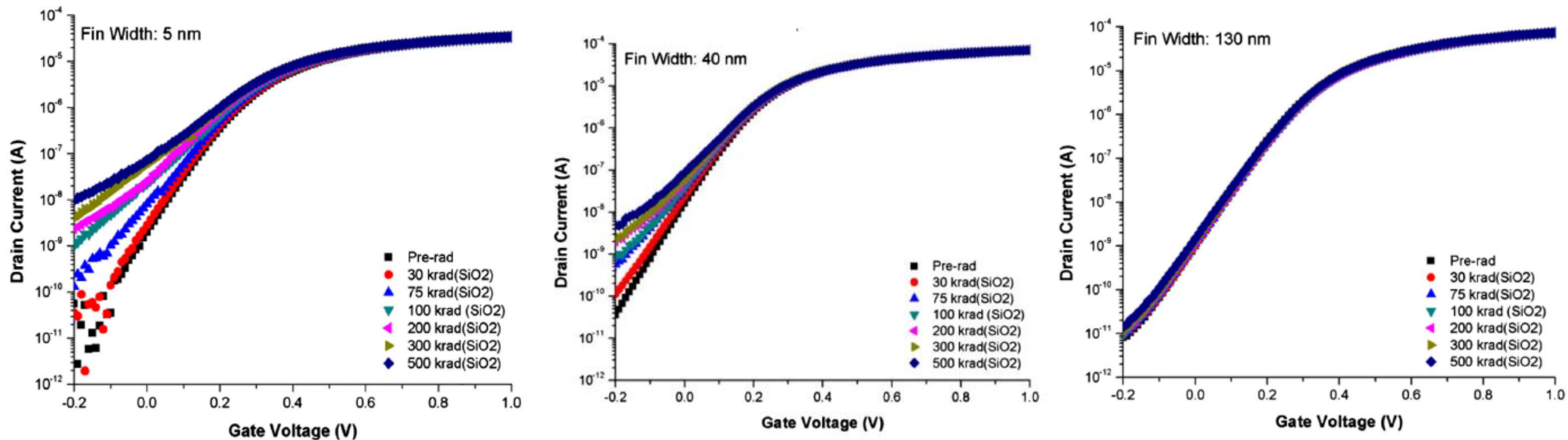
Gate: 5 nm TiN + 100 nm poly-Si

SEG source/drain

Radiation Bulk FinFET – Impact Fin Width

Radiation tolerance increases with increase fin width

Radiation-Induced Narrow Channel Effect (RINCE)

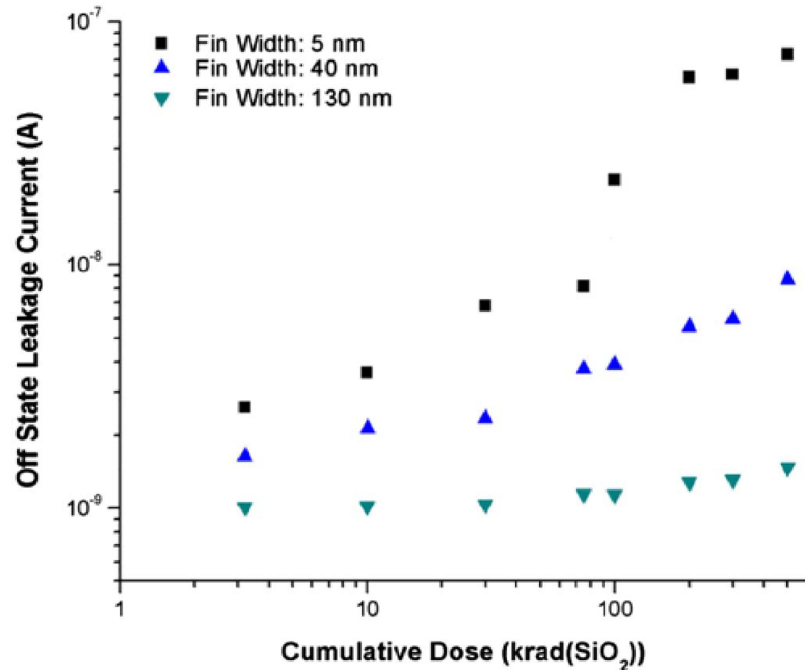


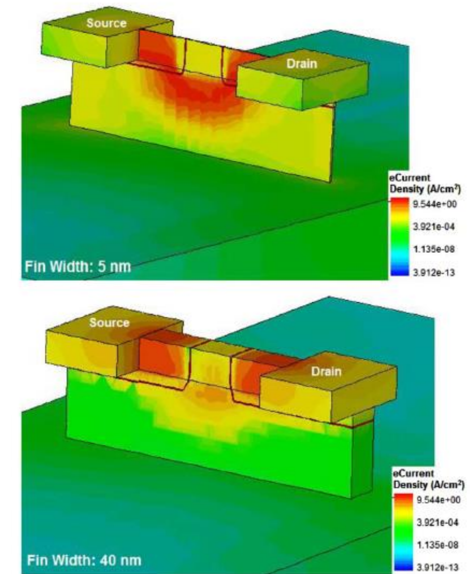
$I_D – V_{GS}$ characteristics as a function of dose for irradiation at a dose rate of 31.5 krad(SiO_2)/min for a 70 nm 5-fin bulk FinFET for three different fin widths. V_{DS} = 50 mV.

I. Chatterjee, E.X. Zhang, B.L. Bhuva, R.A. Reed, M.L. Alles, N.N. Matherme, D.R. Ball, R.D. Schrimpf, D.M. Fleedwood, D. Linten, E. Simoen, J. Mitard and C. Claeys, IEEE Trans. Nucl. Sci., 61, 2951 (2014)

Radiation Bulk FinFET – Impact Fin Width

Off-Current increase for smaller Width and higher dose



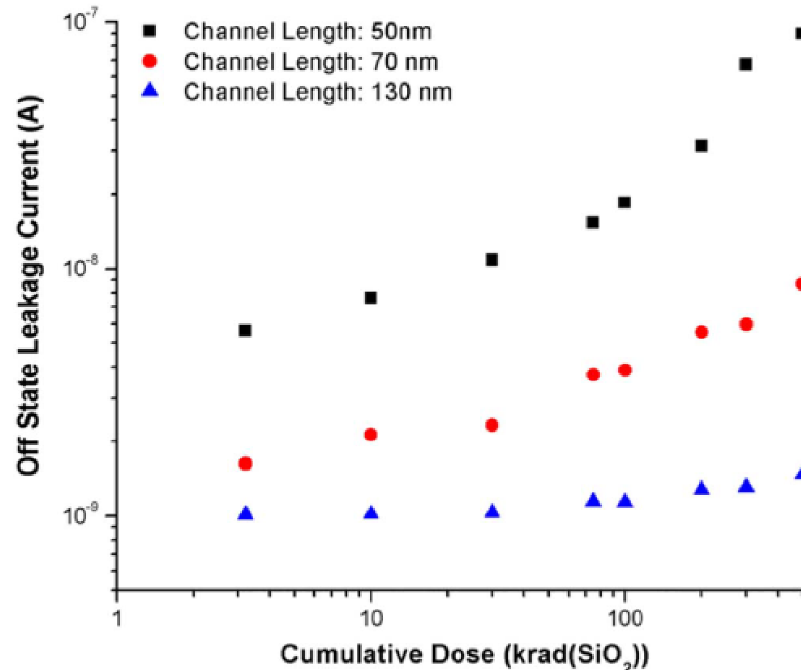


Off-state current (V_{GS} = 0 V) as function of the irradiation dose for a 70 nm 5-fin bulk FinFET with different fin widths. Measurement done at $V_{D.}$

I. Chatterjee, E.X. Zhang, B.L. Bhuva, R.A. Reed, M.L. Alles, N.N. Matherme, D.R. Ball, R.D. Schrimpf, D.M. Fleedwood, D. Linten, E. Simoen, J. Mitard and C. Claeys, IEEE Trans. Nucl. Sci., 61, 2951 (2014)

Radiation Bulk FinFET – Impact Fin Length

Radiation tolerance increases with increasing fin length



Off-state current (V_{GS} = 0 V) as function of the irradiation dose for a 5-fin bulk FinFET with different fin lengths. The fin width is 40 nm. Measurement done at V_{Ds} = 50 mV.

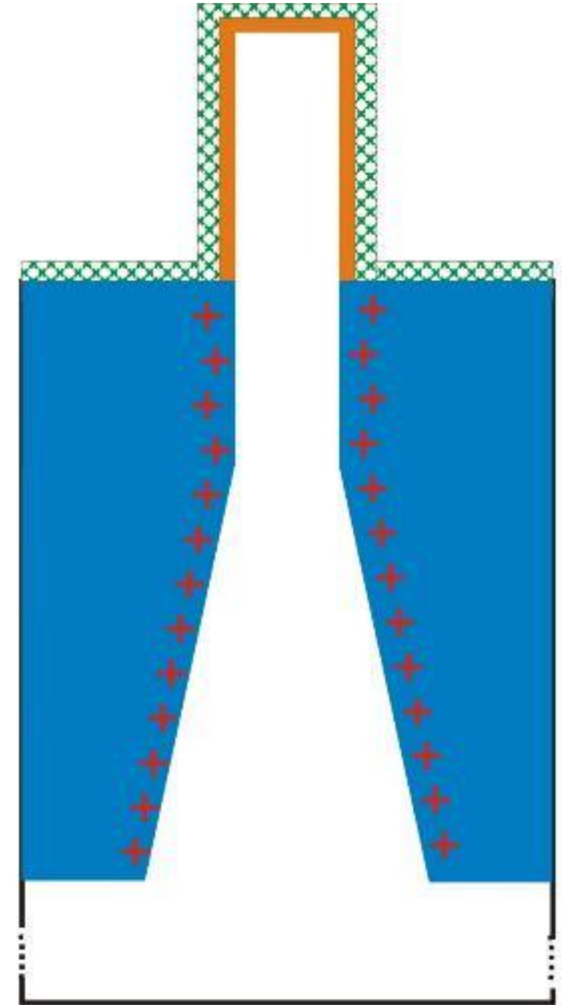
I. Chatterjee, E.X. Zhang, B.L. Bhuva, R.A. Reed, M.L. Alles, N.N. Matherme, D.R. Ball, R.D. Schrimpf, D.M. Fleedwood, D. Linten, E. Simoen, J. Mitard and C. Claeys, IEEE Trans. Nucl. Sci., 61, 2951 (2014)

Bulk FinFETs – Degradation Mechanism

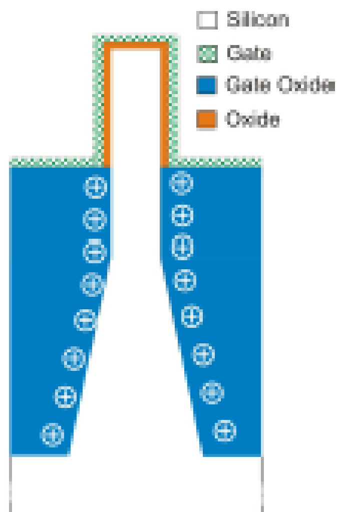
Creation of charges in the shallow trench isolation

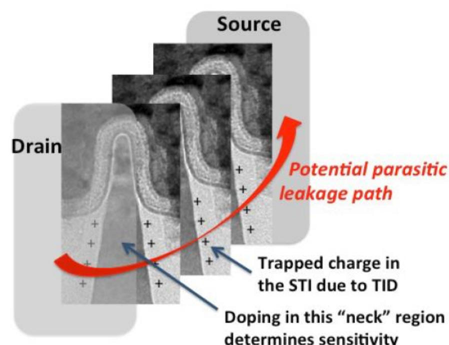
- Positively trapped holes
- PMOS: interface traps also positively charged

Parallel channel in the transistor affected

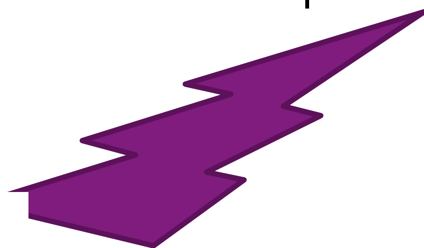


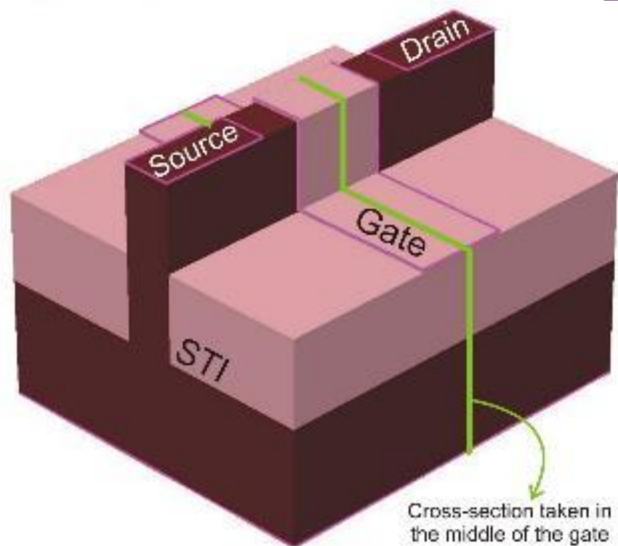
Positive Charge in Bulk FinFET

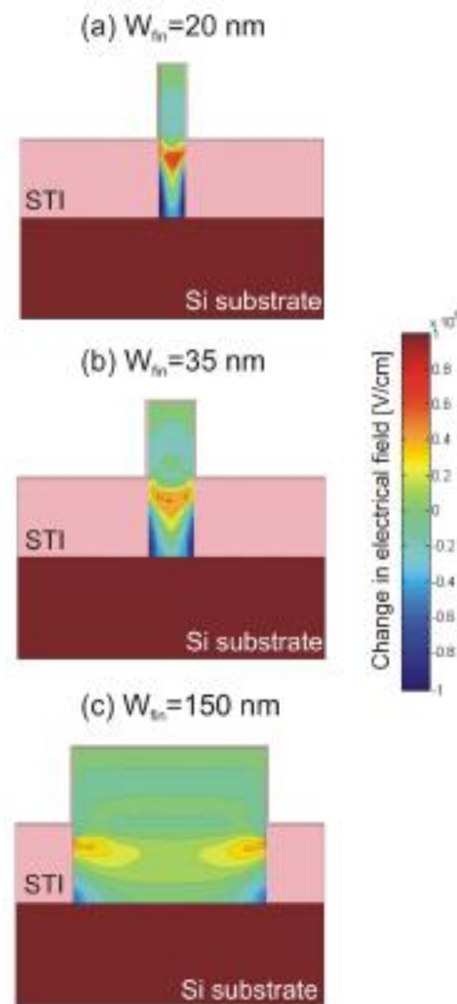




Insert an excess of 10^{12} cm^{-2} positive charge

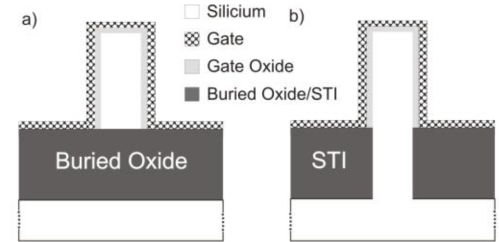


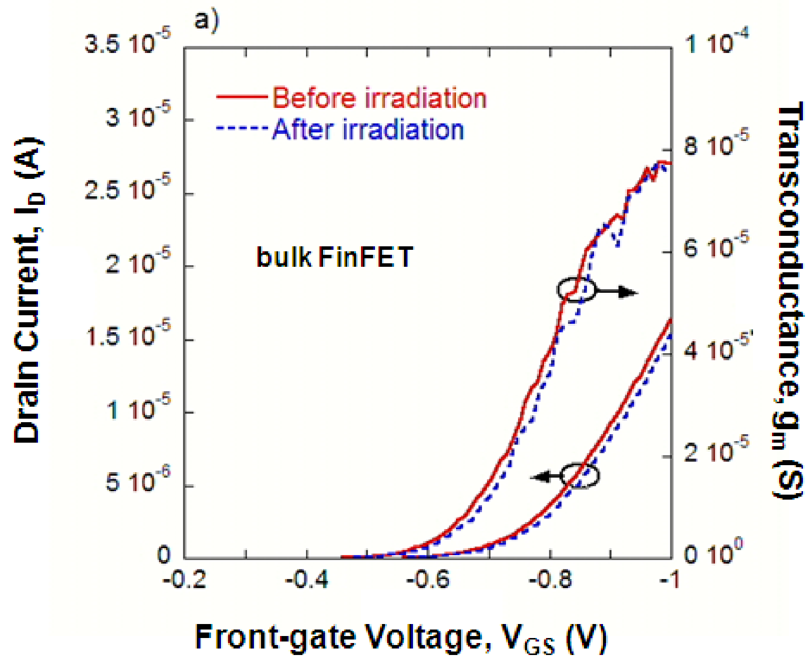


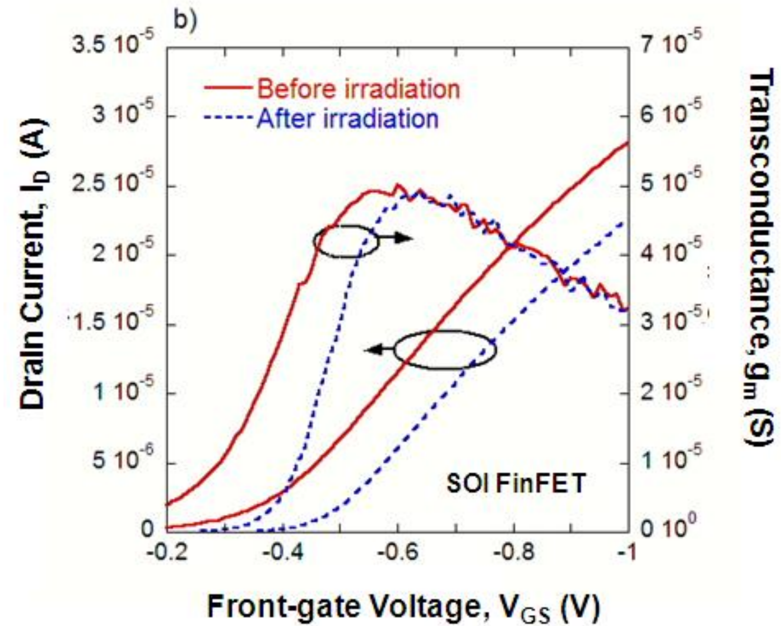


Change in electric field

SOI versus Bulk FinFET





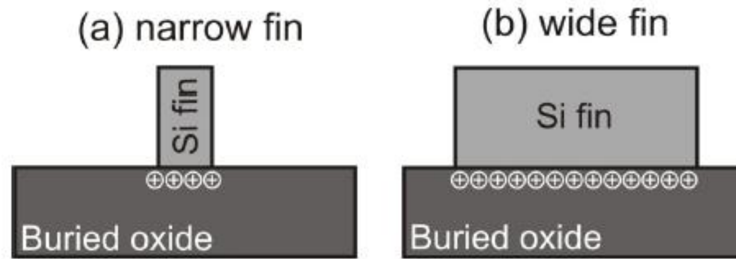


Drain current and transconductance as a function of gate voltage before and after radiation of a bulk (a) and SOI pFinFET (b) with a single fin (W_{FIN} = 885 nm, L= 165 nm, V_{DS}= 50 mV). ^{60}Co irradiation of 10 hours at a dose rate of 1 kGy/hr.

Degradation of wide fin SOI MuGFETs much higher

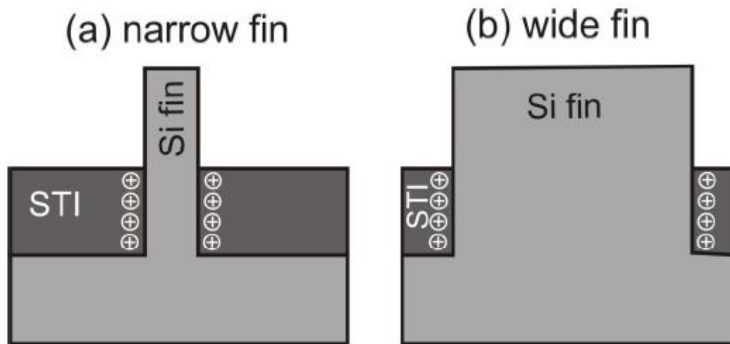
SOI versus Bulk FinFET

SOI



- Degradation increases when fin width increases

Bulk



- Degradation increases when fin width decreases

SOI Different Design Concept

SOI versus Bulk FinFET – Conclusion Gamma Radiation

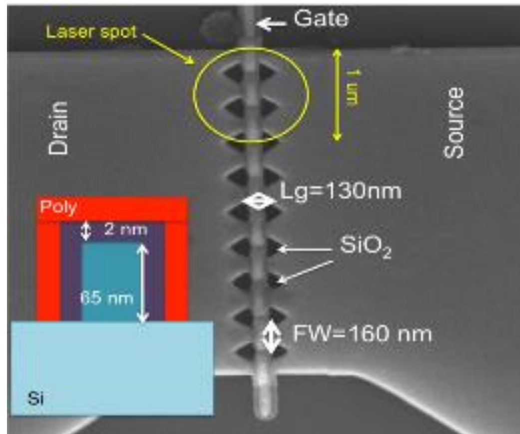
Gamma radiation behavior of bulk pMuGFETs

- **Radiation creates positive charges in the STI**
- **Affects parallel channel in the fin of the MuGFET**

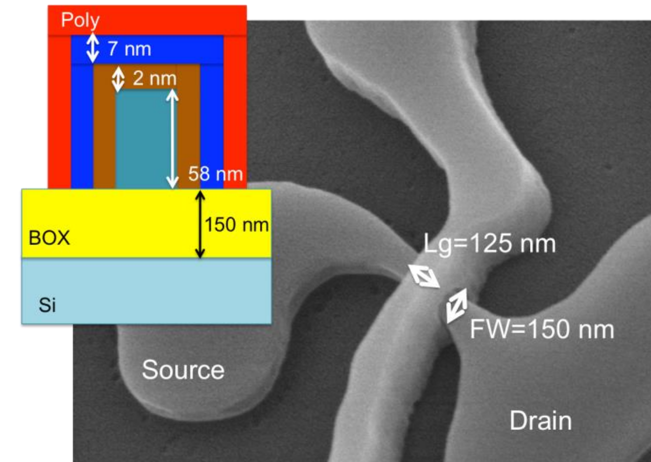
Radiation hardness of bulk pMuGFETs increases when fin width increases

Opposite to behavior of SOI MuGFETs

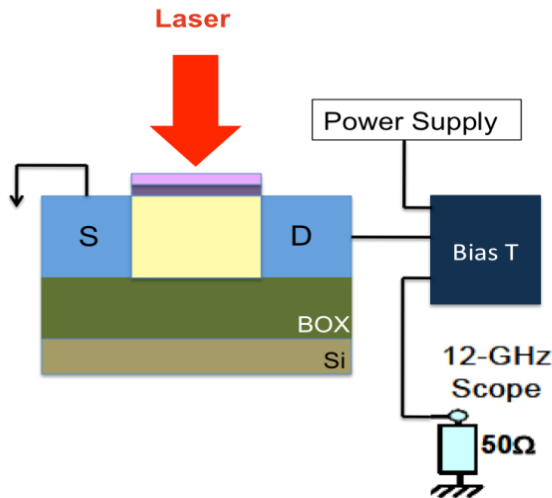
SOI versus Bulk FinFET - SEE
Pulsed Laser Induced Transient Current



Bulk FinFET



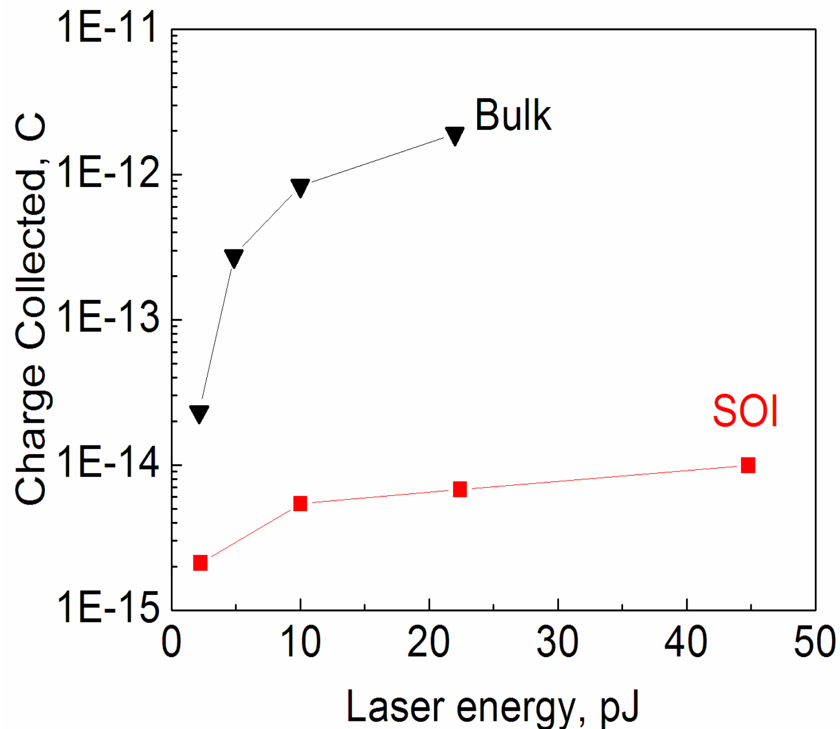
SOI FinFET



Single Photon Absorption (SPA)
- 590 nm
- 1 ps pulse width
- 1 MHz
- about 1 μm spot

F. El-Manouni, R.A. Reed, R.D. Schrimpf, D. McMorrow, E.X. Zhang, K.F. Galloway, E. Simoen, C. Claeys, W. Xiong and S. Cristoloveanu , IRPS conf., Monterey 2011

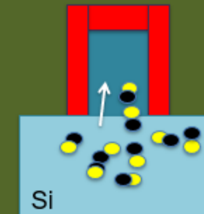
SOI versus Bulk FinFET
Pulsed Laser Induced Transient Current



Semi log curves showing charge collected (C) for bulk (triangles) and SOI (squares) FinFETs as a function of laser energy.

- *Most of the charge collected in the SOI FinFETs was generated in the fins.*
- *Most of the charge collected in bulk FinFETs was generated in the substrate.*

Diffusion in bulk FinFETs

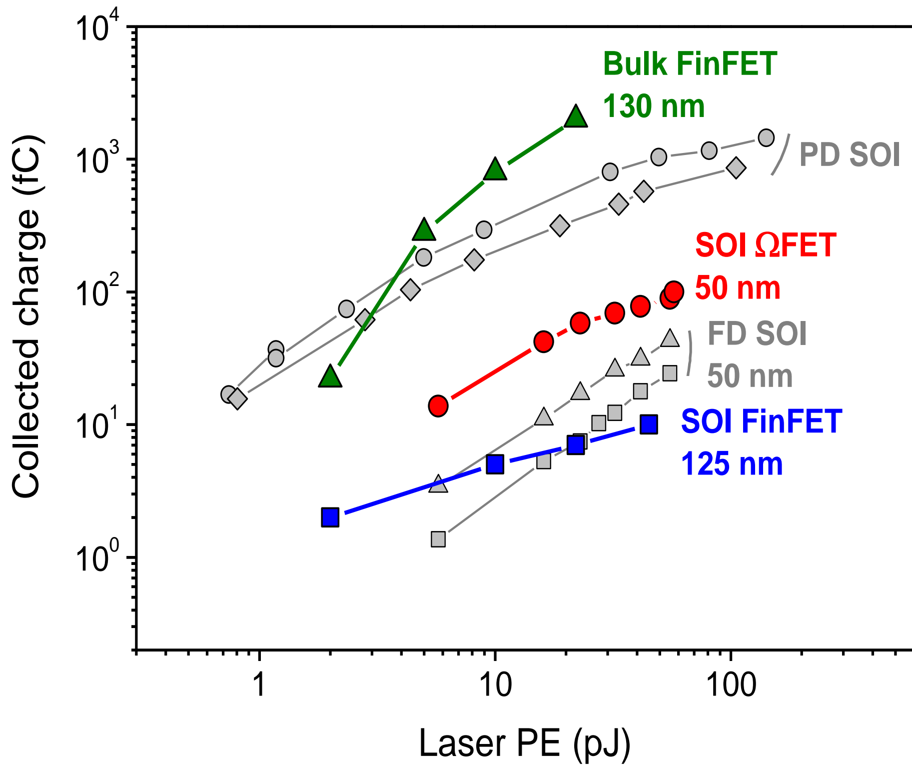


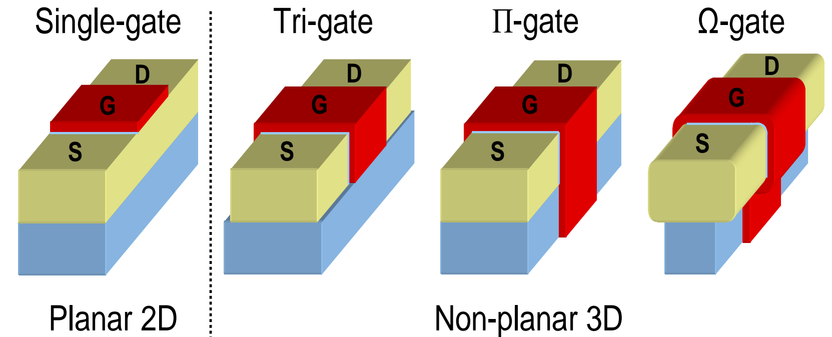
- Carriers diffuse from the substrate to the fin and get collected there in bulk FinFETs. carriers diffusion in SOI samples is prevented thanks to the BOX layer.

SOI FinFETs more suitable to suppress SEE than Bulk FinFETs as the BOX layer isolates the active region from the substrate and consequently reduces the collection volume

F. El-Manouni, E.X. Zhang, R.D. Schrimpf, R.A. Reed, KF. Galloway, D. McMorrow, E. Simoen, C. Claeys, S. Cristoloveanu and W. Xiong, Proc. IRPS Conf., 883 (2011)

Comparison For Different Technologies



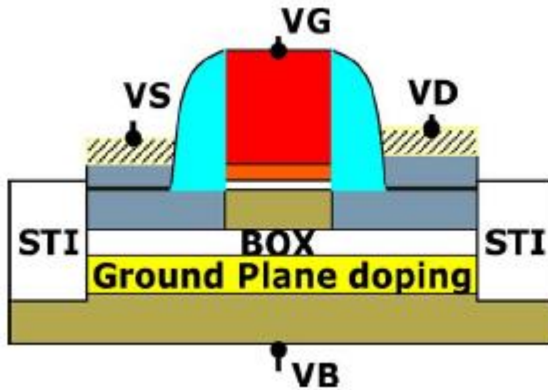


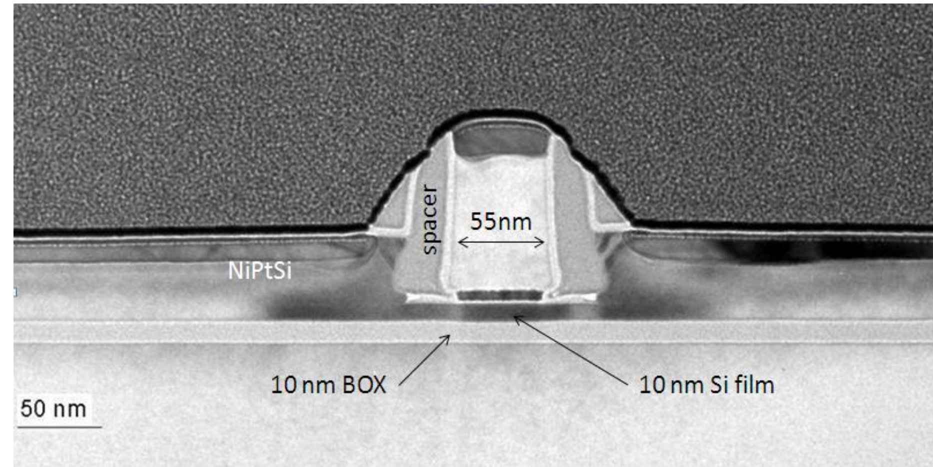
Collected charge vs laser pulse energy (SPA) obtained on several planar single-gate (grey symbols and 3D multiple-gate (colored symbols) technologies.

E. Simoen, M. Gaillardin, P. Paillet, R. Reed, R. Schrimpf, M. Ales, F. El-Mamouni, A. Griffioni and C. Claeys, IEEE TNS, 60, 1970 (2013)

UTBB SOI Devices

UTBB Devices





300 mm

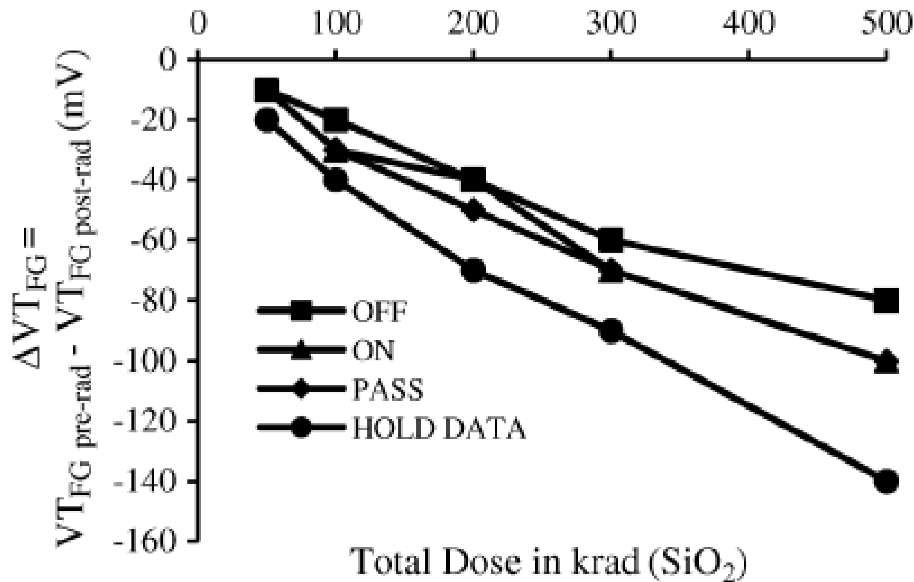
Dielectric: 5 nm SiO_2

Gate: 5 nm PEALD TiN + 100 nm poly-Si

t_{BOX} = 10 nm **t_{Si} = 10 or 20 nm**

- **Thin BOX positive effect.**
- **Thin Si film increases coupling front- and back-interface.**

UTBB Devices

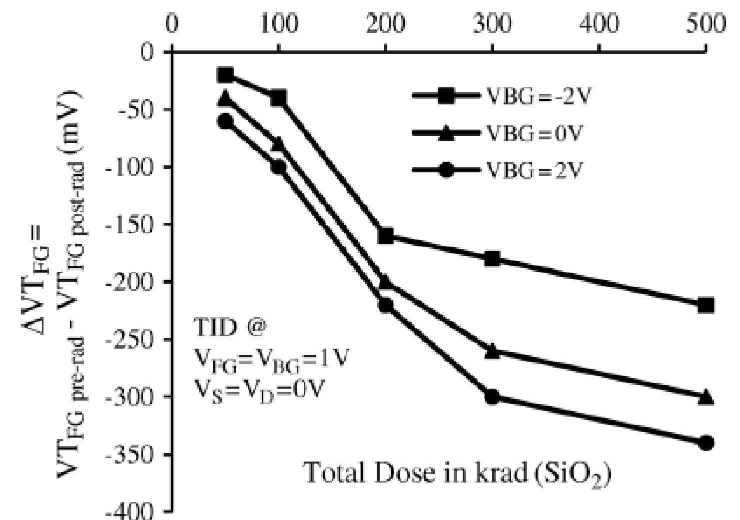


IRRADIATION BIAS CONDITIONS

V_{FG} (V)	V_{BG} (V)	V_D (V)	V_S (V)	Bias
1	0	0	0	ON
0	0	1	0	OFF
0	1	1	1	PASS
1	1	0	0	HOLD DATA for FBRAMs

V_T shifts front-gate transistor under different bias conditions. Max V_T shift for HOLD DATA bias (front and back positive bias).

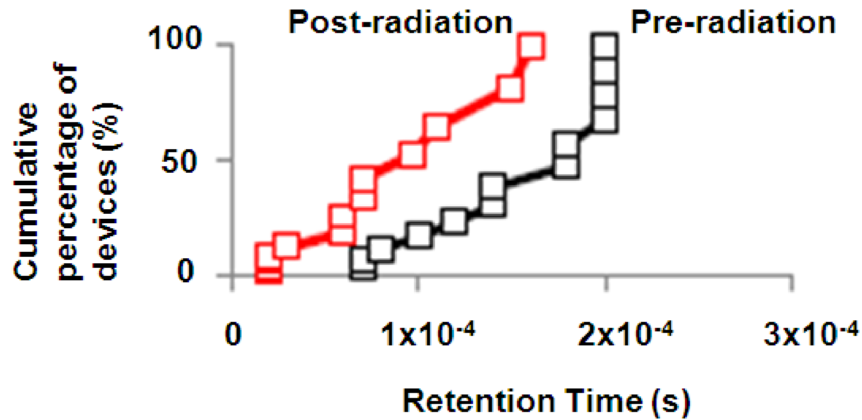
Effect back-gate bias



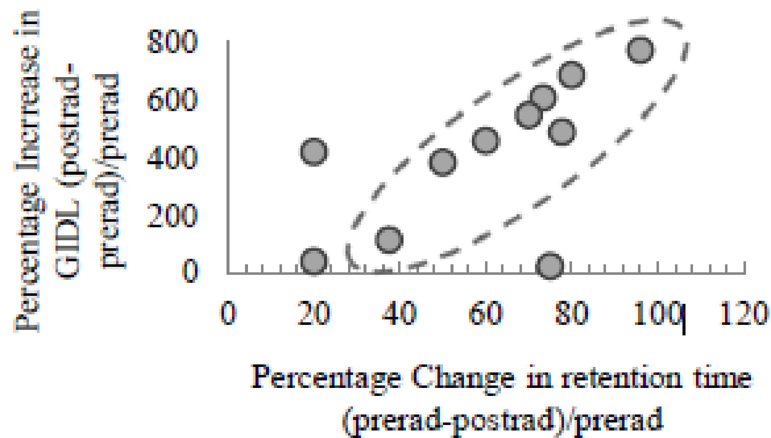
Lower shift for lower V_B. This increases the retention time of 1T- FBRAM cells.

N. N. Mahatme, E. X. Zhang, R. A. Reed, B. L. Bhuva, R. D. Schrimpf, D. M. Fleetwood, D. Linten, E. Simoen, A. Griffoni, M. Aoulaiche, M. Jurczak, and G. Groeseneken, IEEE Trans. Nucl. Sci., 59 2966 (2012)

Performance – Retention Time



Retention time distribution of 13 1-T FB UTBOX cells.



N.N. Mahatme *et al*., presented at NSREC 2012

Conclusions FinFETs and UTBB SOI

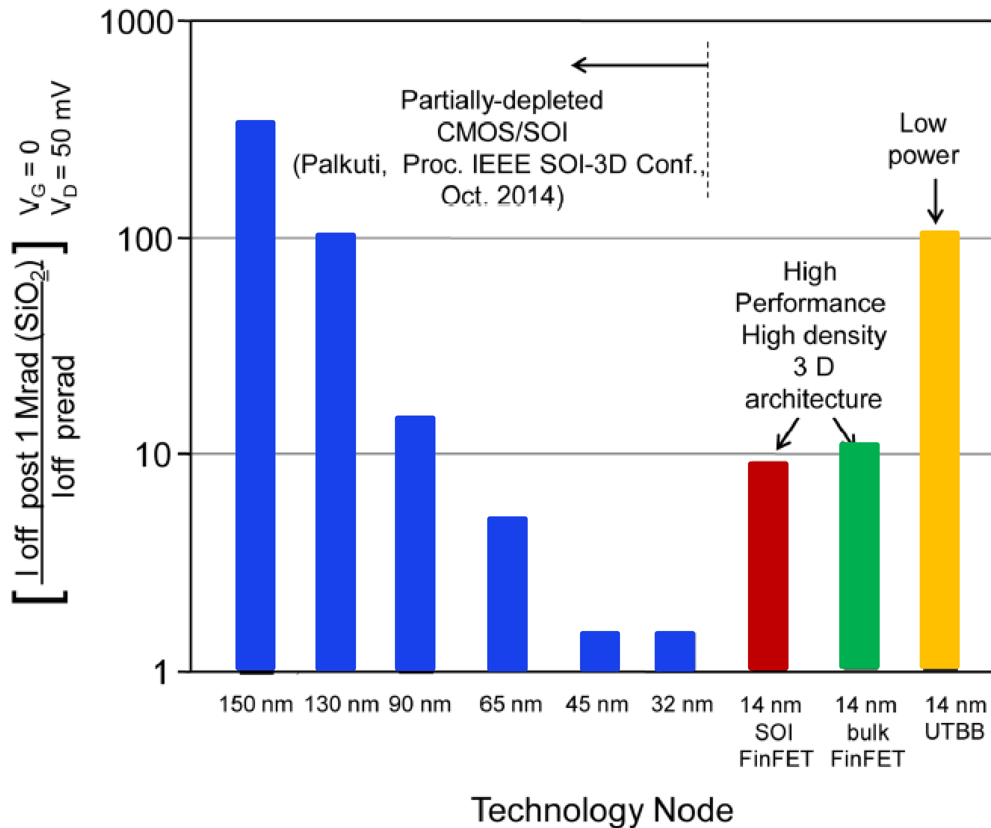
- Positive trapped charge in the BOX triggers the back-channel n-transistor, increasing the gm. Leads to a turn-off of the p-channel.

- Strong impact of the back-channel voltage on the radiation performance.

- Different radiation-hard design for SOI and Bulk FinFETs

- The thin buried oxide makes FDSOI devices more tolerant to radiation. Due to strong coupling effects between both interfaces, any radiation-induced degradation at one interface affects the other interface, so the quality of the Si/BOX interface must be carefully controlled.

Radiation Hardness SOI – Scaling Trend



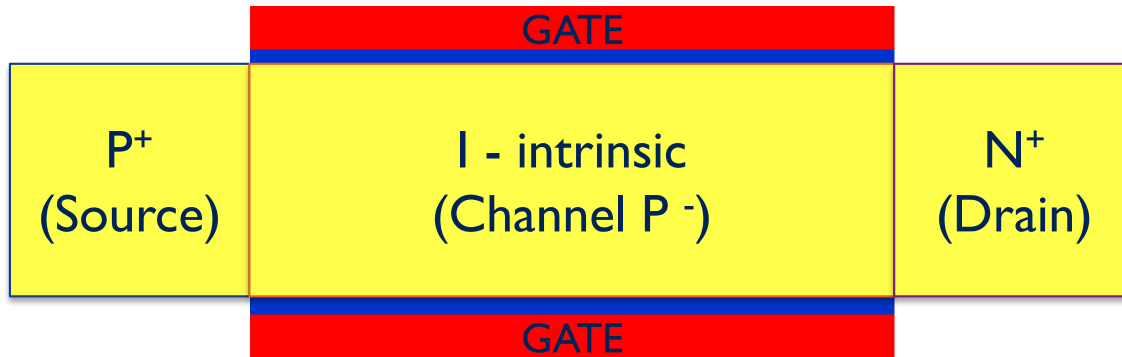
- Reduced channel doping
- Isolation oxide, spacers
- Different architecture

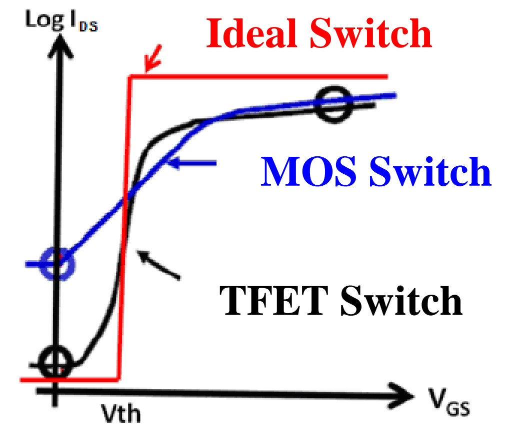
Commercial Technology TID response of off-state current for a dos of 1 Mrad (SiO2) versus technology scaling showing vulnerability turnaround after 32 nm

H. Hughes, P. McMarr, M. Alles, E. Zhang, C. Arutt, B. Doris, D. Liu, R. Southwick and P. Oldiges, 2015 IEEE Radiation Effects Data Workshop (REDW))

TunnelFETs

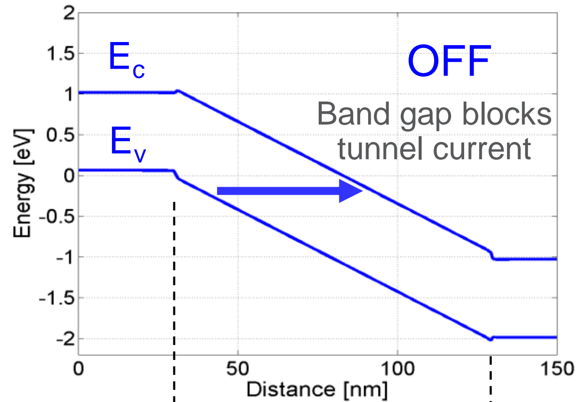
TunnelFET (TFET)

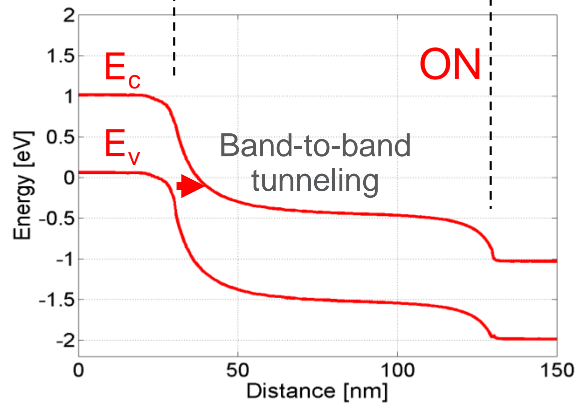




- **Based on PIN Diode technology**
- **Reduced short-channel effects**
- **Lower subthreshold swing**
  - **Due to different mechanism of conduction: Tunneling**
  - **May be less than 60 mV/dec**

nTunnelFET – Band Gap



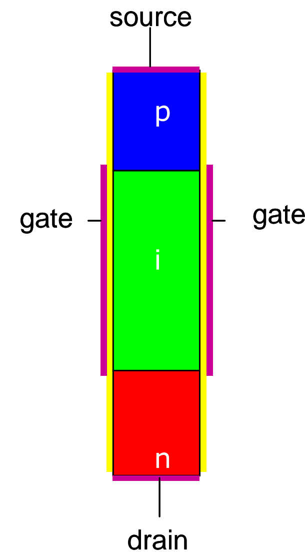


OFF

$V_G = 0V$

ON

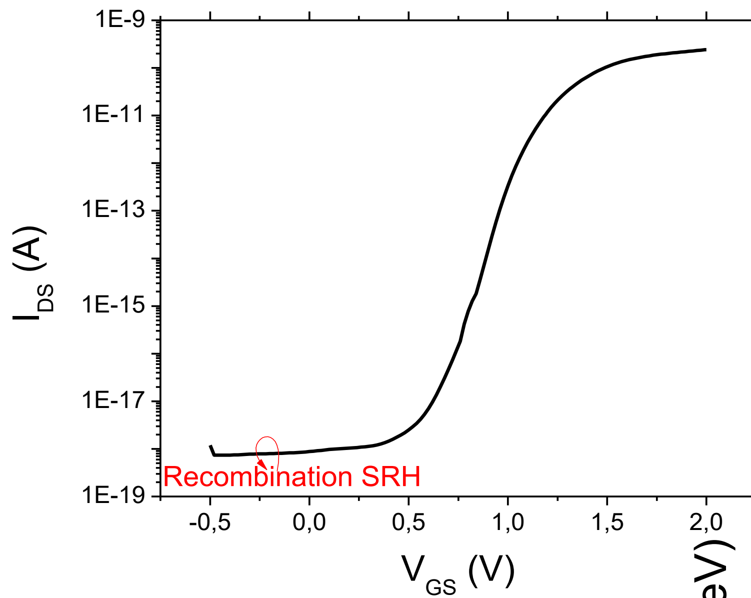
$V_G > 0V$

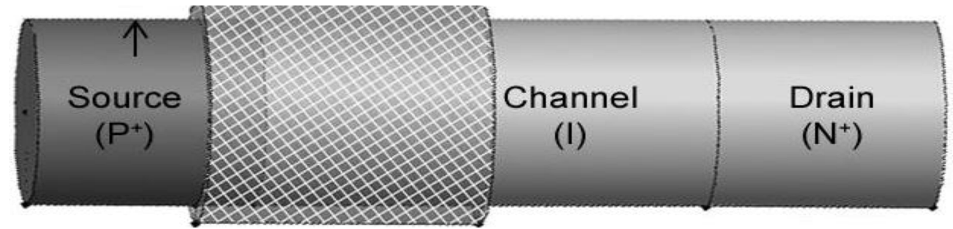


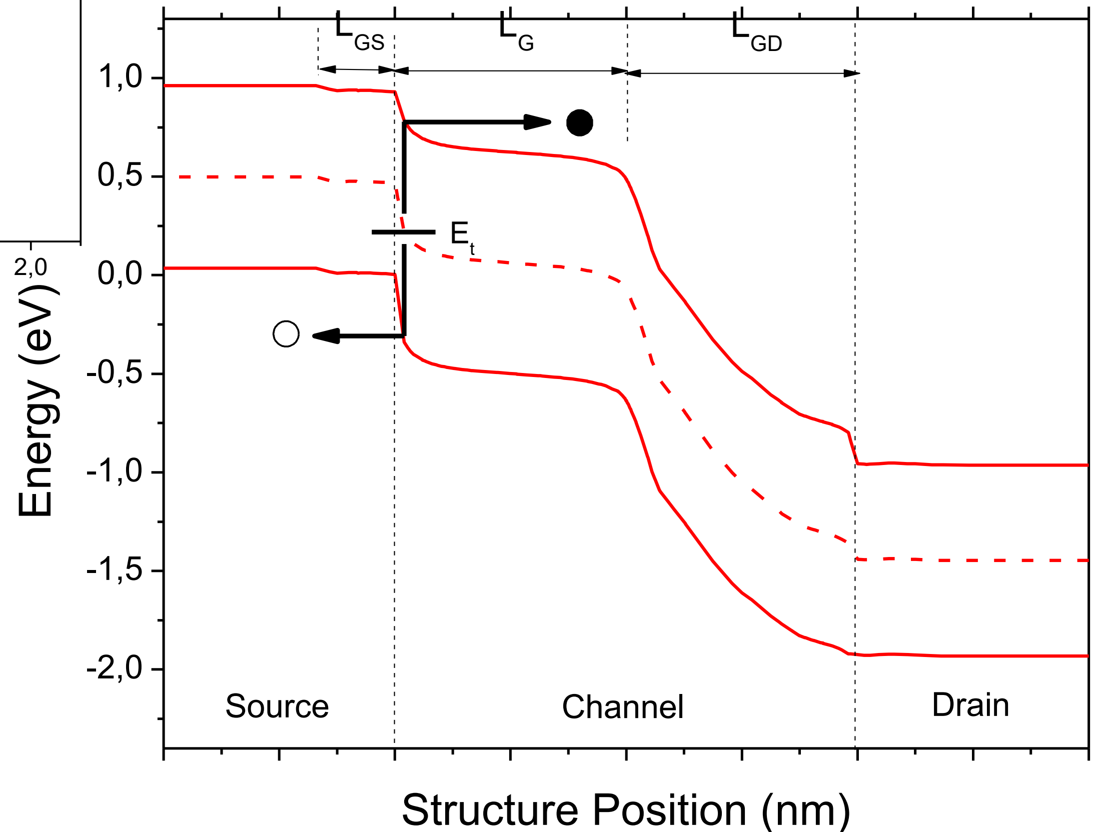
Low I_{OFF}, Low V_{DD}

SS<60mV/decade

TFET - Conduction Mechanism

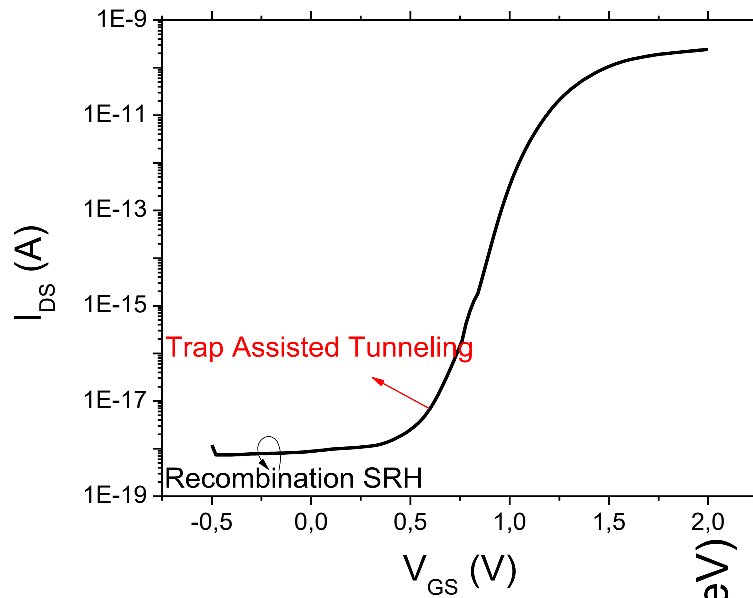


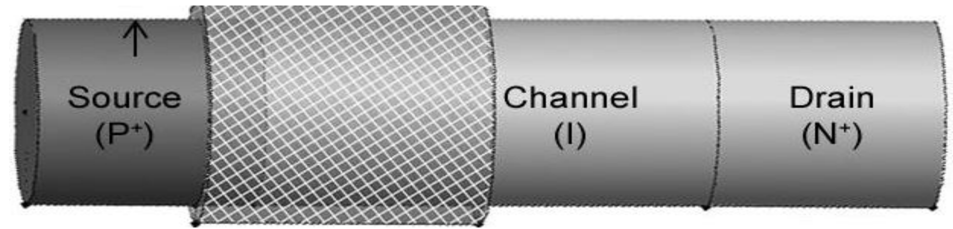


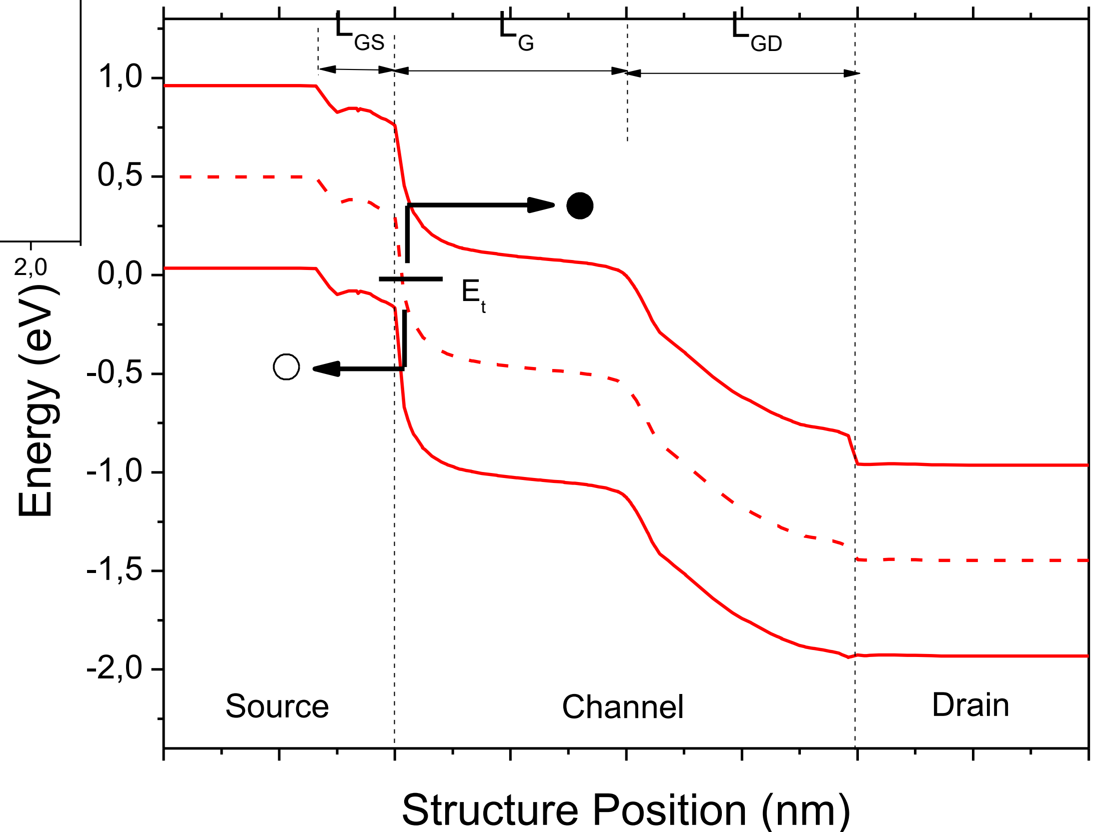


$$J_{SRH} \propto C_1 . e^{\left(-\frac{\frac{E_g}{2} + \Delta E_t}{k.T}\right)}$$

TFET - Conduction Mechanism

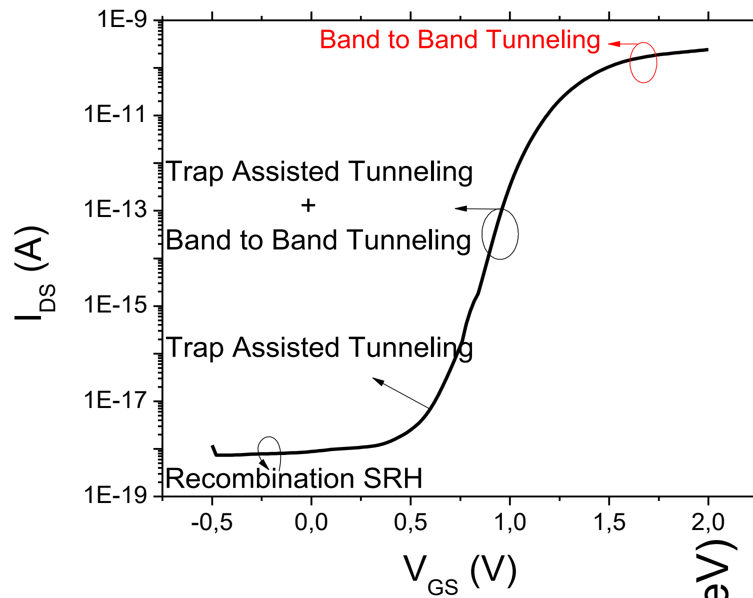


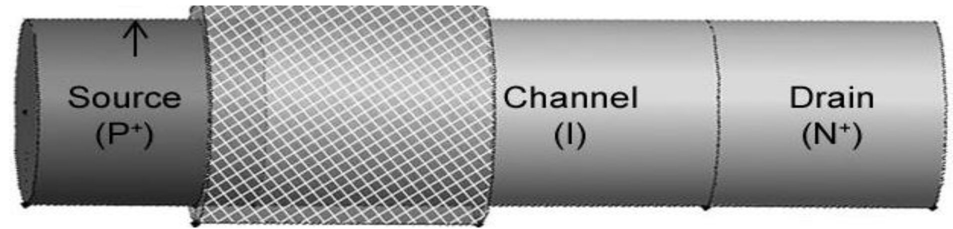


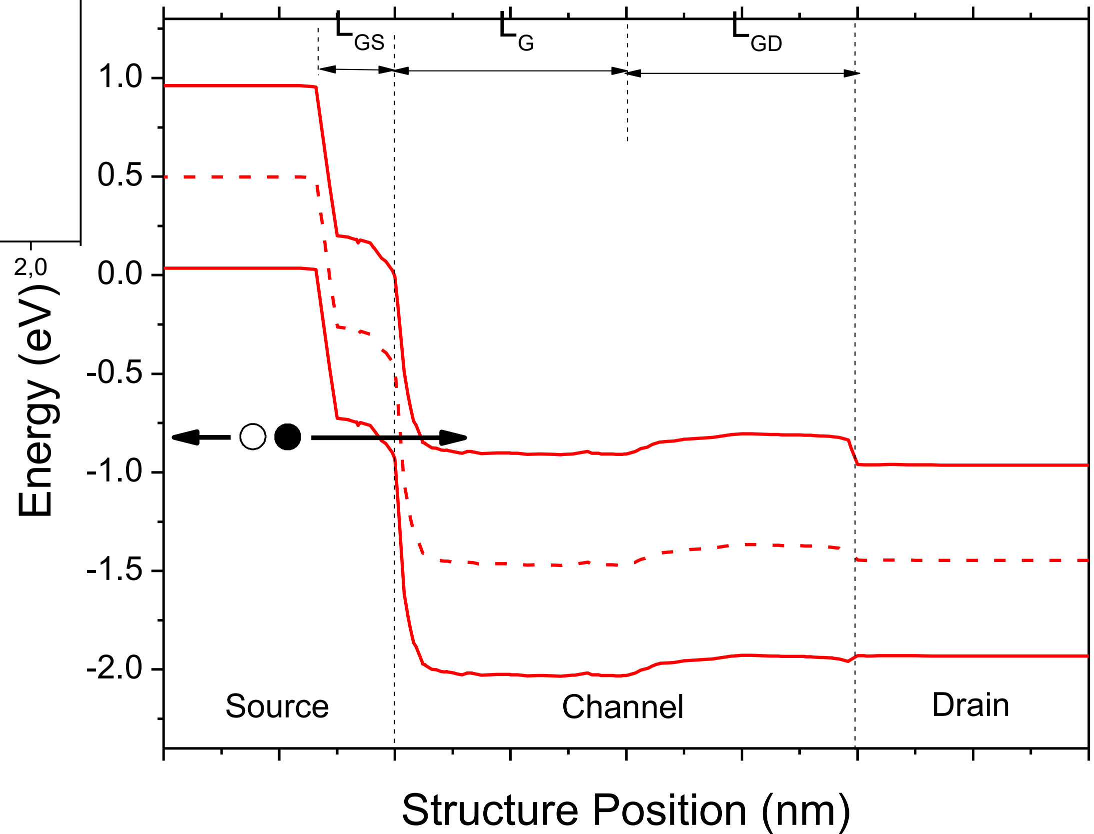


$$J_{TAT} \propto C_2 . e^{\left(-\frac{\frac{E_g}{2} + \Delta E_t}{k.T}\right)}$$

TFET - Conduction Mechanism







$$J_t \propto e^{\left(-C_3 . \frac{E_g{}^{3/2}}{\xi}\right)}$$

Choice TFET Material

- tunneling probability ~ $(E^2 m_r^{1/2} . E_g^{-0.5}) \exp(-A. E_g^{1.5})$

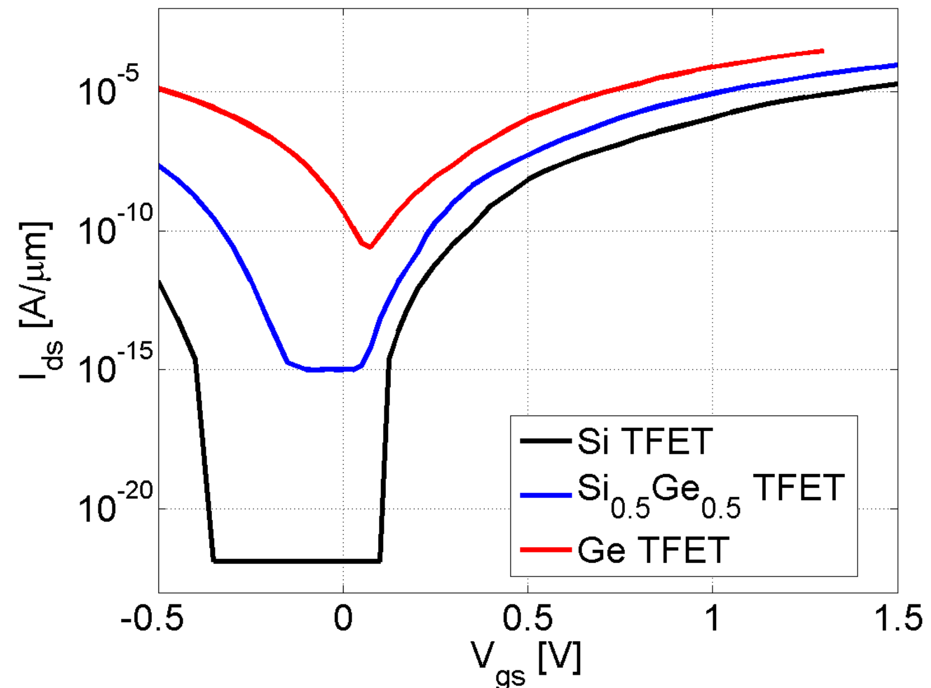
  $E_{g,Si}$ = 1.12 eV

  $E_{g,Ge}$ = 0.66 eV

- - *I-V* curves show:

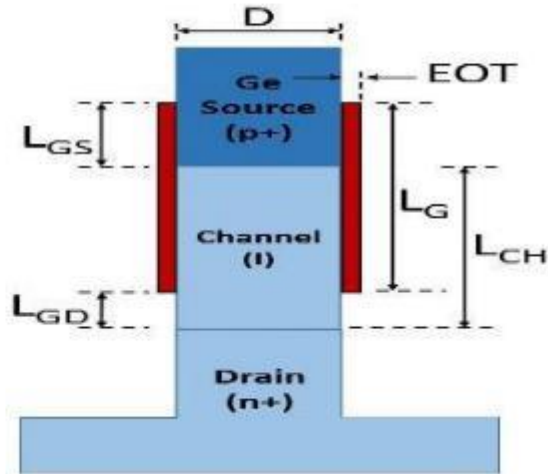
  $I_{ds,Ge} \approx 100\ I_{ds,Si}$

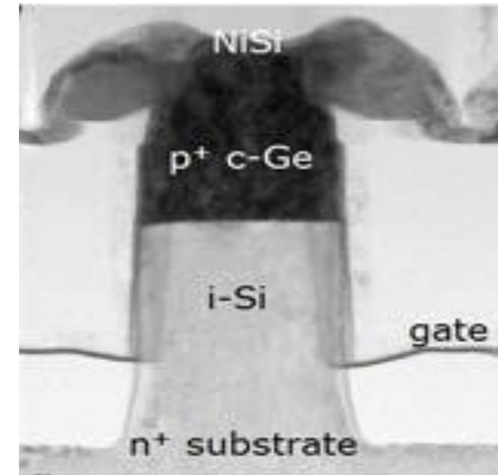
- smaller bandgap improves tunneling, but want silicon-based TFET…

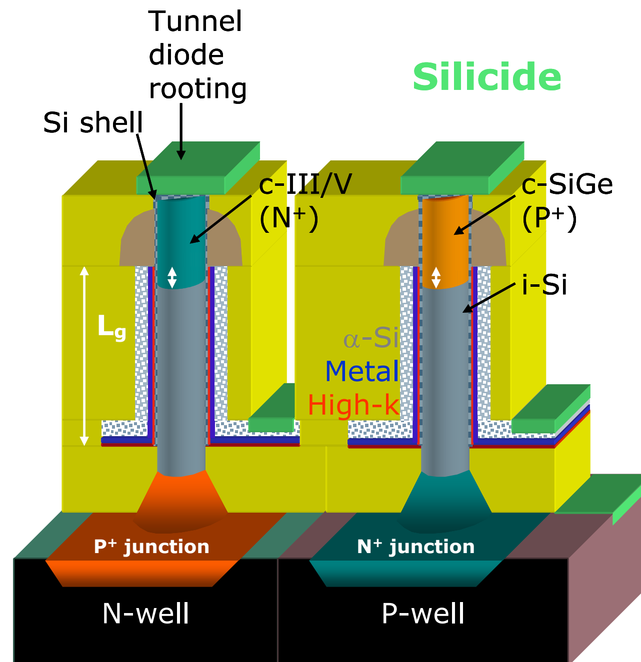


Remark: Ge TFET-curve is shifted to the left for easier comparison

Hetero-structure TFET

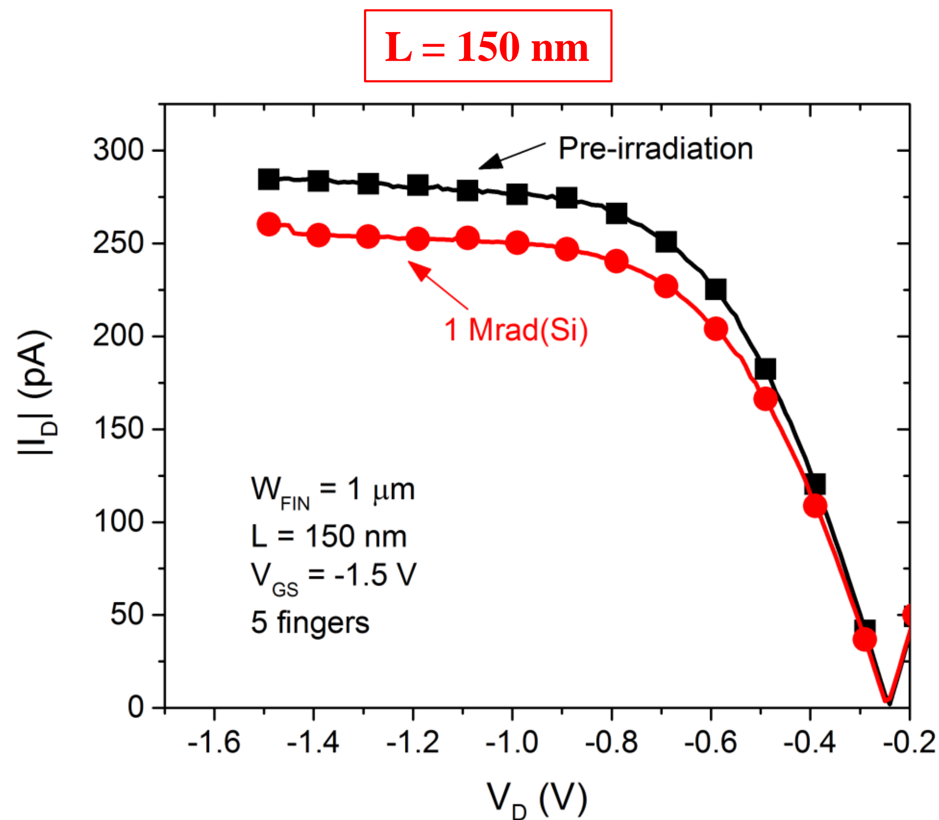


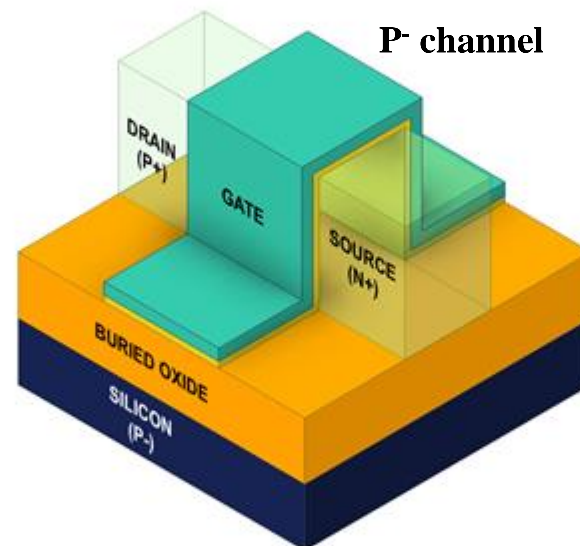




Radiation SOI p-TFETs

L = 150 nm





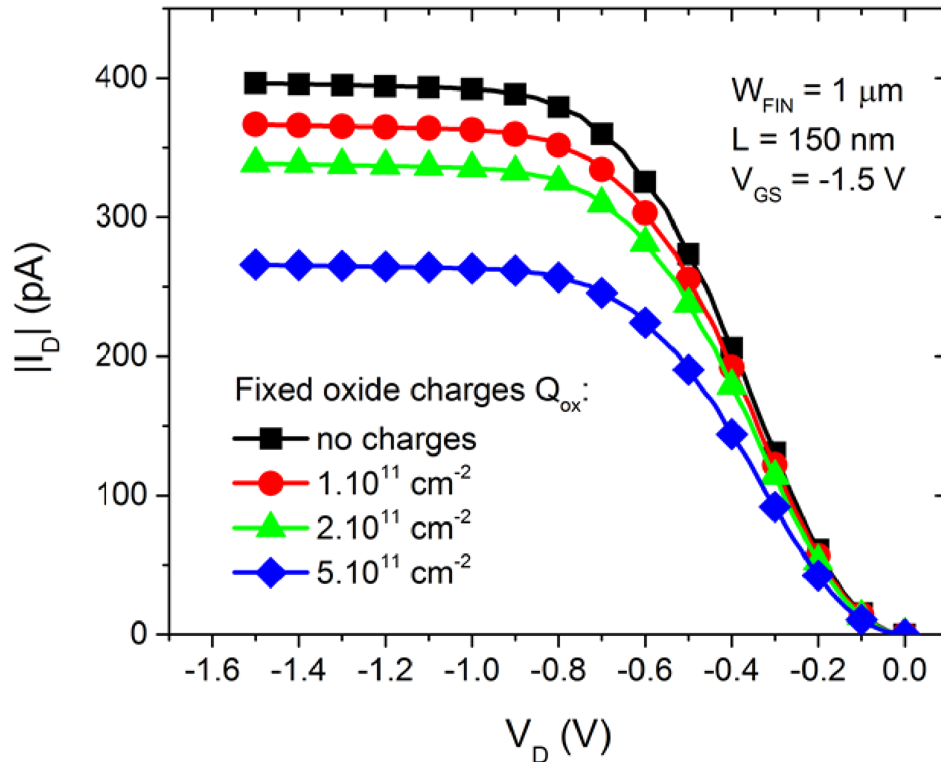
Pre- and post-irradiation (1 Mrad(Si) protons) drain current as a function of drain voltage for a W = 1 μm, L = 150 nm pTFET device.

About 10% reduction in drain current for L = 150 nm

H.L.F. Torres, J.A. Martino, R. Rooyackers, A. Vandooren, E. Simoen, C. Claeys and P. G. D. Agopian, Proc. SBMicro 2017

Radiation SOI p-TFETs - Simulation

Charge sheet at the front- and back interface

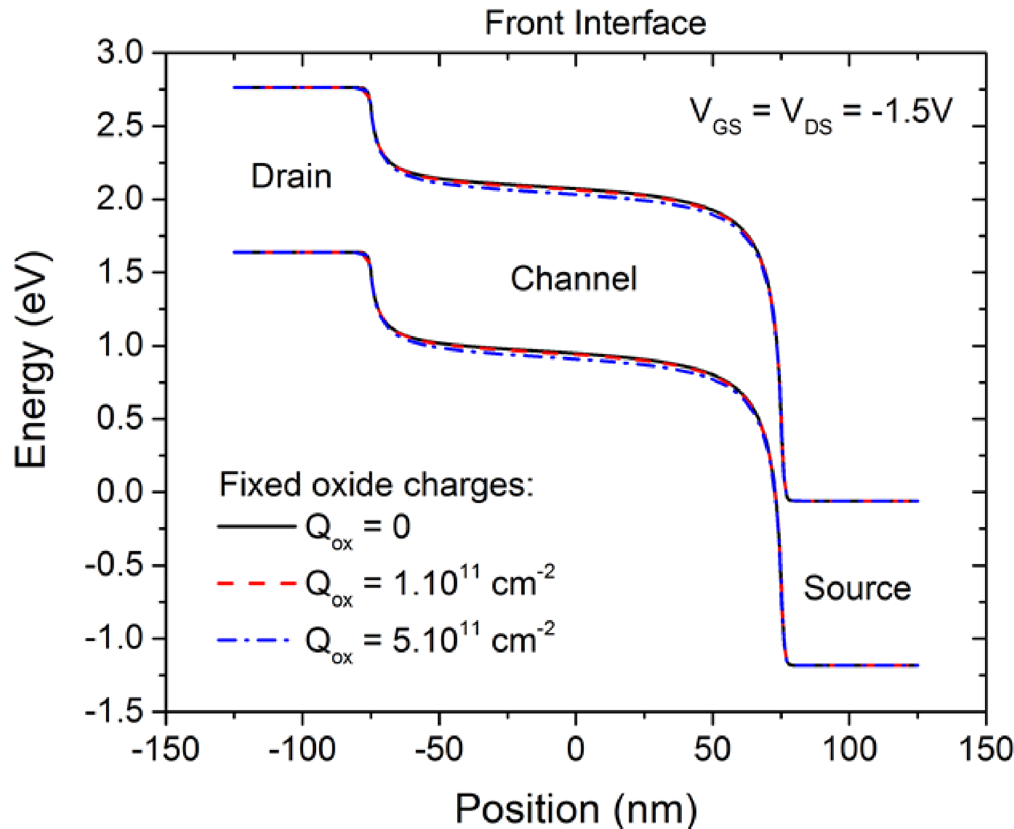


Output characteristic of a simulated W/L = 1/0.15 µm pTFET considering fixed charges at front and back interface

H.L.F. Torres, J.A. Martino, R. Rooyackers, A. Vandooren, E. Simoen, C. Claeys and P. G. D. Agopian, Proc. SBMicro 2017

Radiation SOI p-TFETs - Simulation

Charge sheet at the front- and back interface



Front interface energy bands diagram along device channel for different fixed oxide charges conditions

- **Only slight shift in the channel region**
- **Strong impact on the current due to the exponential dependence of the tunneling probability: Increase ON current**

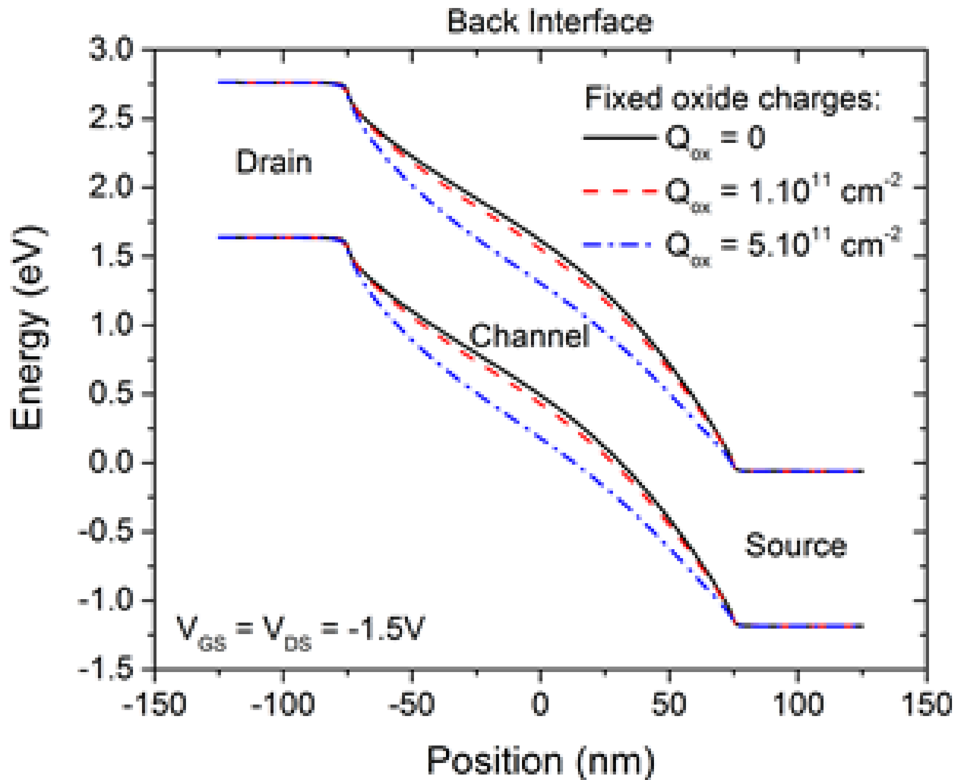
$$T_{BTBT} = exp\left(-\frac{4\lambda\sqrt{2m^* E_g^3}}{3qh\left(E_g + \Delta\Phi\right)}\right)$$

- **Radiation-induced charges reduce the surface potential and thus the tunneling probability**

H.L.F. Torres, J.A. Martino, R. Rooyackers, A. Vandooren, E. Simoen, C. Claeys and P. G. D. Agopian, Proc. SBMicro 2017

Radiation SOI p-TFETs - Simulation

Charge sheet at the front- and back interface



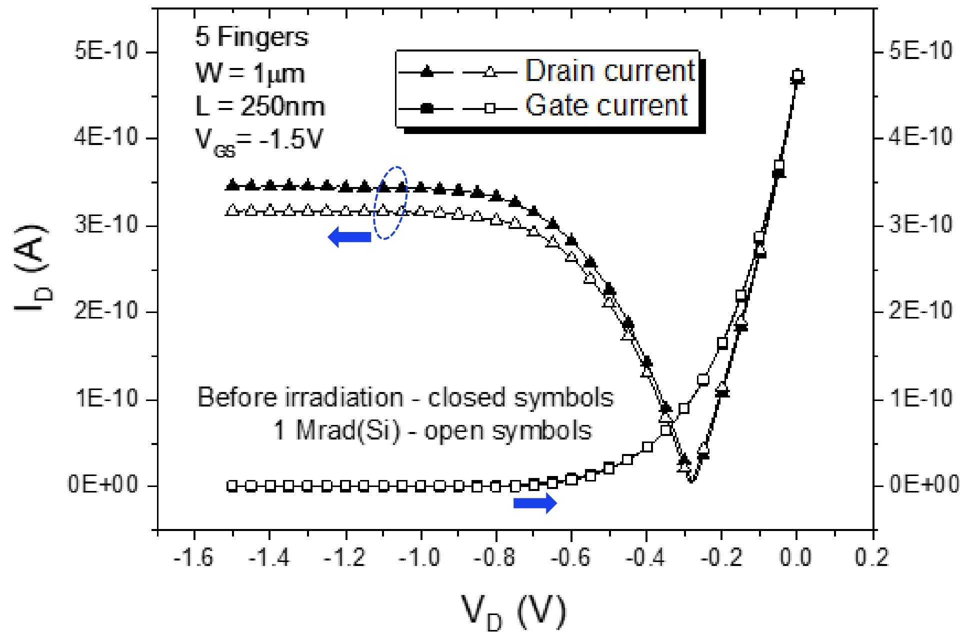
- Strong shift in the channel region

Back interface energy bands diagram along device channel for different fixed oxide charges conditions

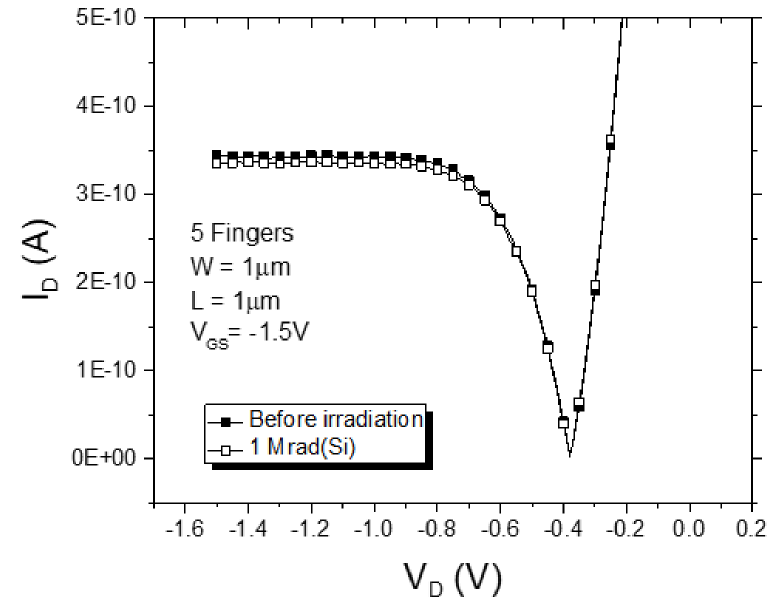
H.L.F. Torres, J.A. Martino, R. Rooyackers, A. Vandooren, E. Simoen, C. Claeys and P. G. D. Agopian, Proc. SBMicro 2017

Radiation SOI p-TFETs – Length Impact

L = 250 nm



L = 1μm

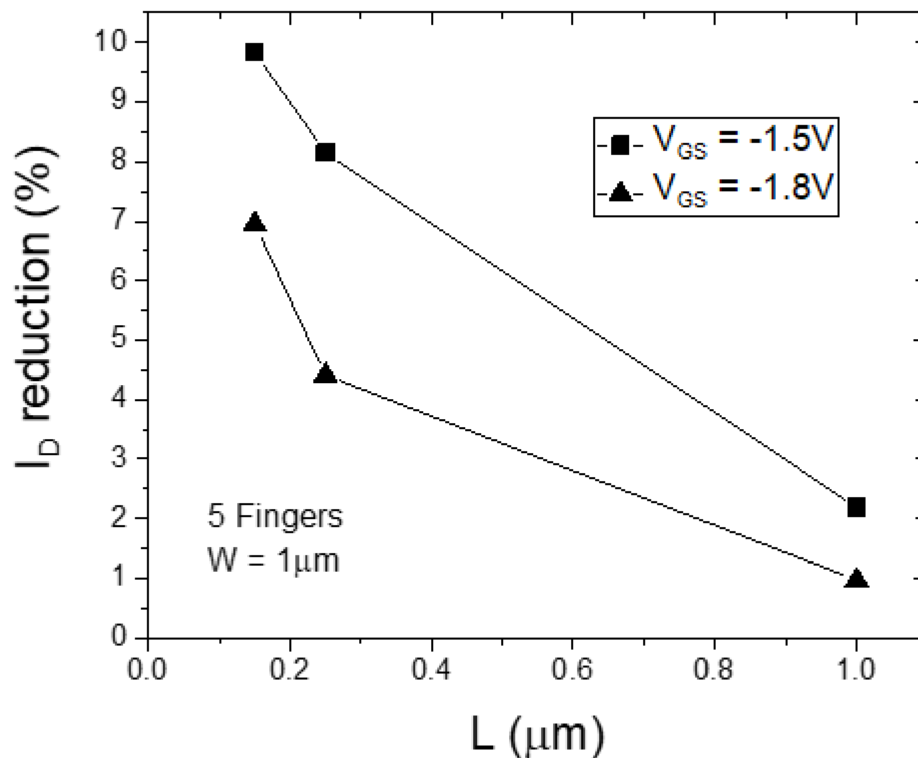


Drain current as a function of drain voltage for a W = 1μm pTFET device

About 8% reduction in drain current for L = 250 nm and 2% for L= 1 μm

H.L.F. Torres, J.A. Martino, R. Rooyackers, A. Vandooren, E. Simoen, C. Claeys and P. G. D. Agopian, Proc. SBMicro 2017

Radiation SOI p-TFETs



On-current reduction due to the irradiation as a function of channel length

Long channel length: Increased channel resistance

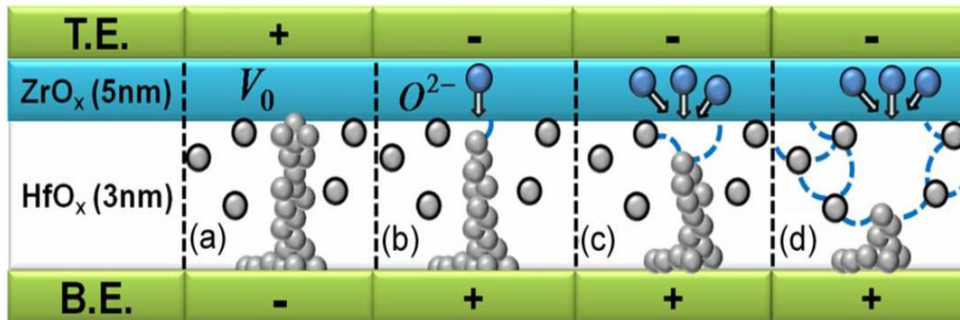
Increased channel resistance reduces the back tunneling current → **Reduced I_{on}**

H.L.F. Torres, J.A. Martino, R. Rooyackers, A. Vandooren, E. Simoen, C. Claeys and P. G. D. Agopian, Proc. SBMicro 2017

Resistive Memories (ReRAMs)

Radiation Resistive Memories (ReRAMs)

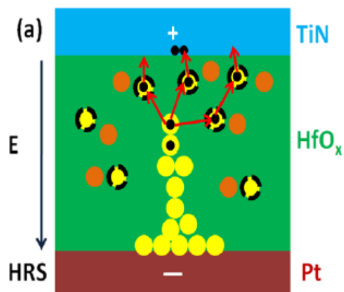
Valence Change Memory (VCM)

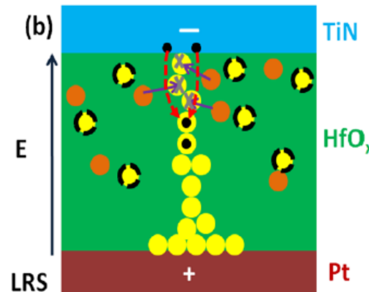


(a) The conducting path is generated by applying the positive SET voltage during LRS. (b) The conducting path is oxidized by oxygen migration due to the application of the RESET voltage. (c) and (d) The oxidized region expands as the negative RESET voltage is increased.

D. Lee, J. Lee, M. Jo, J. Park, M. Siddik and H. Hwang, IEEE Electron Device Lett., 32, 964, (2011)

- **Concentration oxygen vacancies is important**
- **Radiation can break Hf-O bonds resulting in more oxygen vacancies**





Upon cycling after radiation, the radiation [V] in HfO*x* , located far from the filament, are not recovered, and therefore lead to an average decrease of HRS resistance. When in HRS [as shown in (a)], with a partial filament present, the induced oxygen vacancies aid connection of the filament upon SET. When in LRS [(b)], nonlattice oxygen can recombine with oxygen vacancies in the filament and cause rupturing.

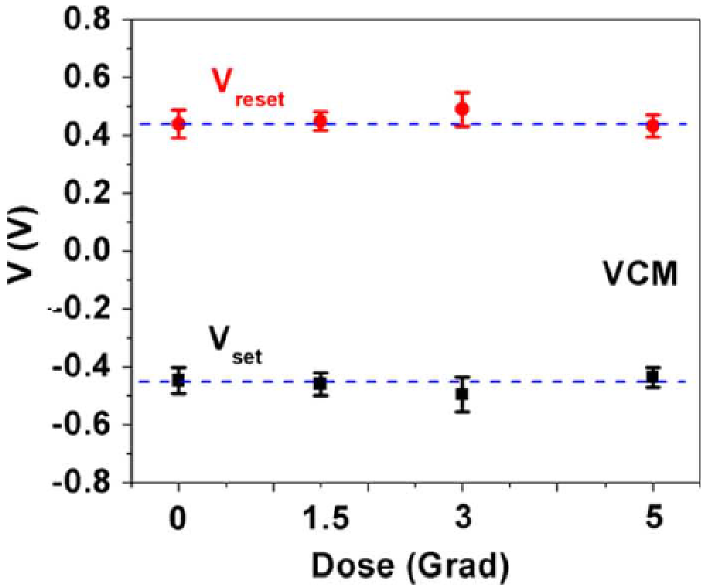
R. Fang, Y. Gonzalez Velo, W. Chen, K.E. Holbert, M.N. Kozicki, H. Barnaby and S. Yu. Appl. Phys. Lett. 104, 183507 (2014)

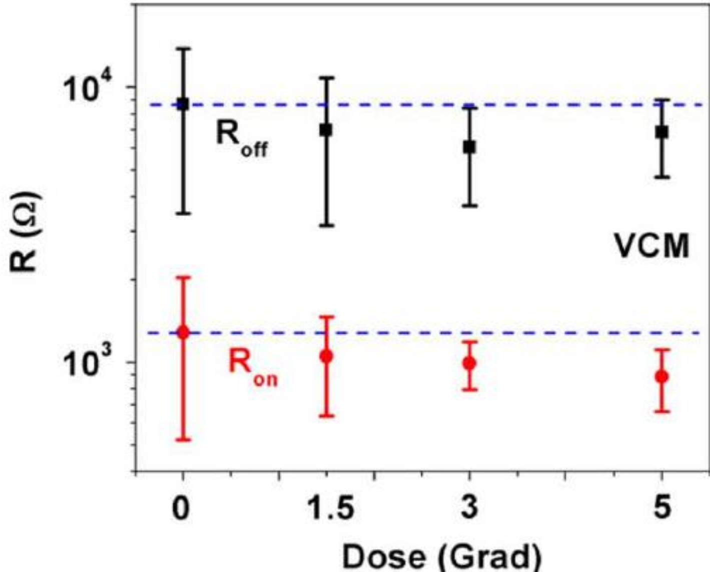
Proton Radiation Hardness Resistive Memories (ReRAMs)

Valence Change Memory (VCM)

Very Hard

TiN/HfO_2(20 nm)/TiN
200 krad/s at a H^+ ion energy of 1 MeV





(left) Average V_{set} (in black) and Vreset (in red and (right) average R_{off} (in black) and R_{on} (in red) of all devices at three total doses in VCM ReRAMs. The dashed lines are used as a visual reference to average pre-radiation values

- Radiation has no impact on V_{set} and V_{reset}
- R_{off} and R_{on} decrease slightly for high dose radiation

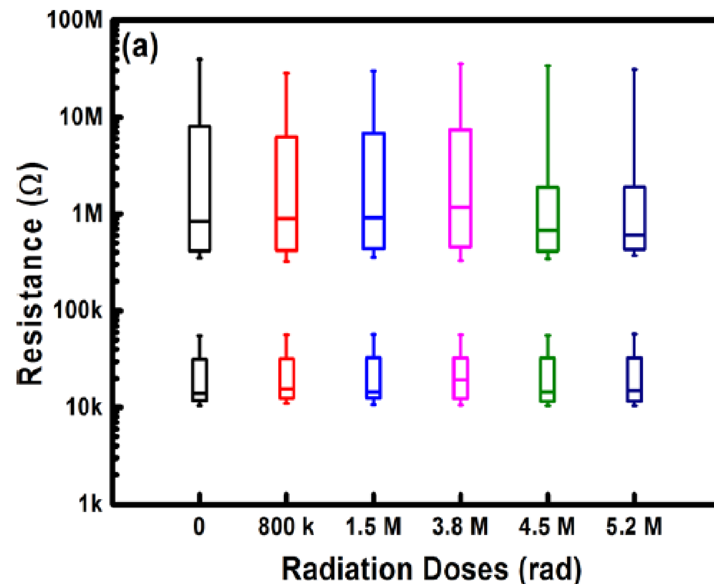
H. Xiaoli, W. Wei, B, Butcher, S. Tanachutiwat and R.E. Geer, IEEE Trans. Mucl. Sci. 59, 2550 (2012)

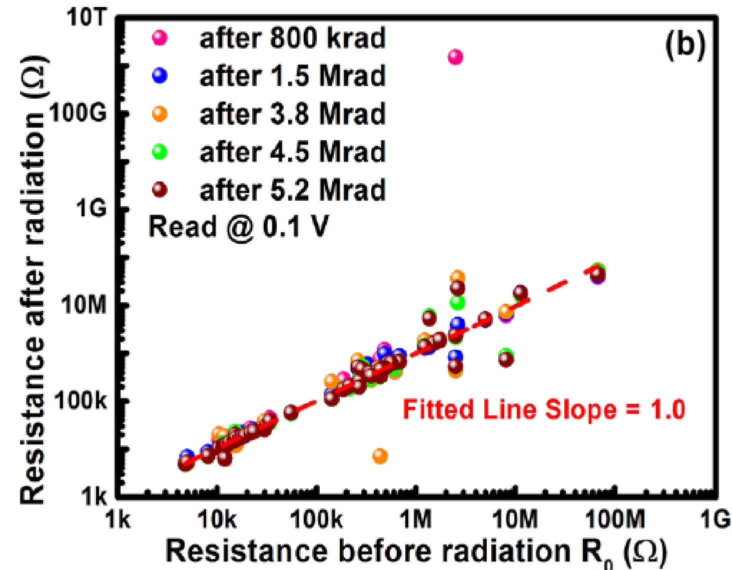
γ-Radiation Hardness Resistive Memories (ReRAMs)

Valence Change Memory (VCM)

TiN(50 nm)/HfO_x(10 nm)/Pt(50 nm)

Very Hard





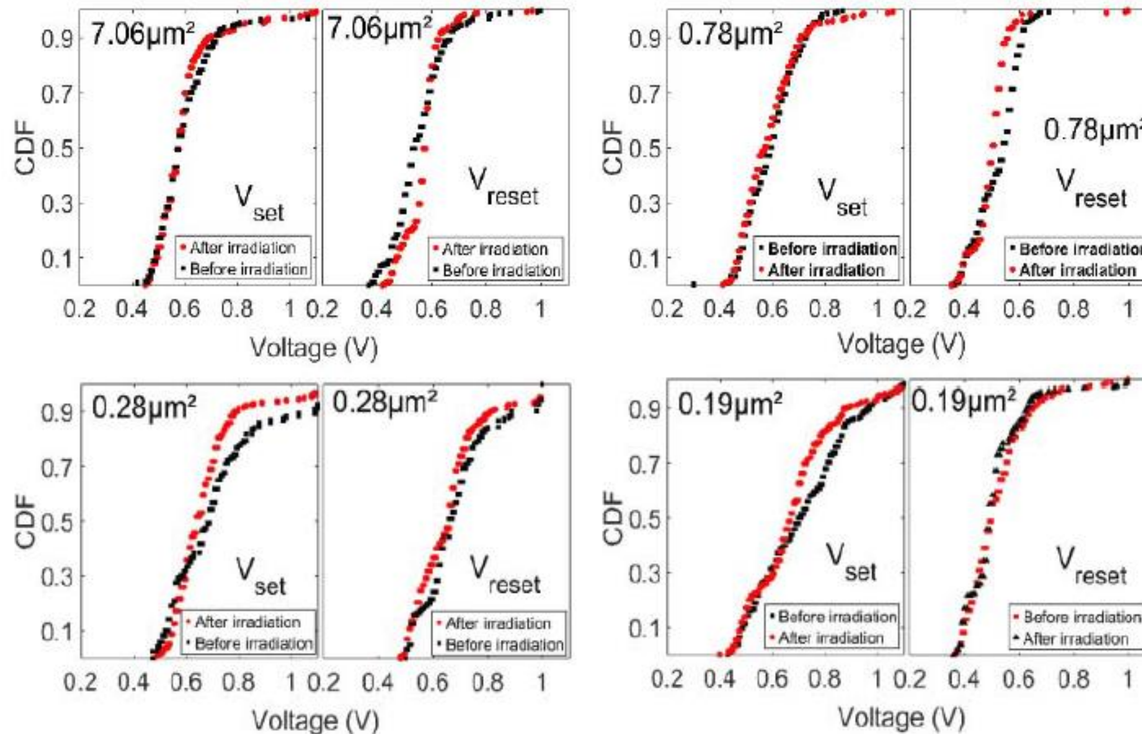
(a) Resistance states evolution with different c-ray doses for 20 samples of 55 lm2 (the upper edge of the box shows the 75% of the distribution, and lower edge shows the 25% of the distribution).
(b) Resistance comparison before and after irradiation for all the 60 samples.

R. Fang, Y. Gonzalez Velo, W. Chen, K.E. Holbert, M.N. Kozicki, H. Barnaby and S. Yu. Appl. Phys. Lett. 104, 183507 (2014)

I-Ion Radiation Hardness Resistive Memories (ReRAMs)

Valence Change Memory (VCM)

TiN(10 nm)/HfO_x(5 nm)/TiN(35 nm)



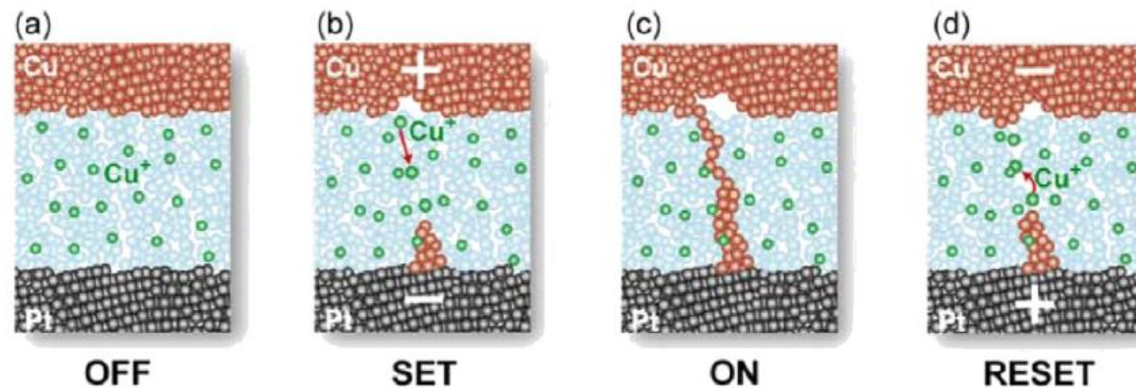
Very SSE Hard

Cumulative probability distribution of the set and reset voltages for cells with different sizes, before and after irradiation with iodine up to a fluence of $2.2 \cdot 10^9$ cm^{-2}. These cells were irradiated in both HRS and LRS state

M. Alayan, M. Bagatin, S. Gerardin, A. Paccagnella, L. Larcher, E. Vianello, E. Nowak, B. De Salvo and L. Perniola, IEEE Trans. Nucl. Sci. 64, 2018 (2017)

Radiation Hardness Resistive Memories (ReRAMs)

Electrochemical metallization memory (EMC)
Programmable metallization cells (PMC)
Conductive-bridge random access memory (CBRAM)
Cation-based devices



During the OFF state, the Cu-doped ECM cell has no filaments present. During the SET operation, the Cu ions from the top electrode dissolve into the switching layer to Cu^+ and a filament is formed at the counter electrode (Pt) due to the applied bias.This continues until a complete metallic filament connects the top and bottom electrodes, resulting in the ON state. The process can be reversed by changing the applied bias, causing the filament to rupture (RESET).

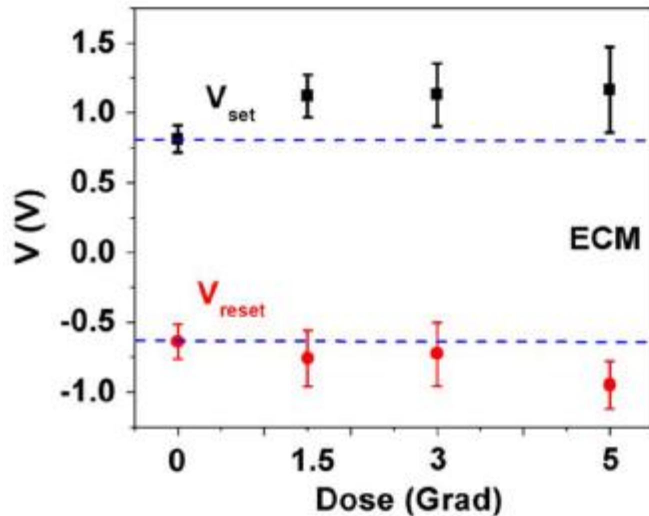
Radiation-induced vacancies in the ECM ReRAMs inhibit the formation of the metallic filament through internal field reduction due to charge trapping

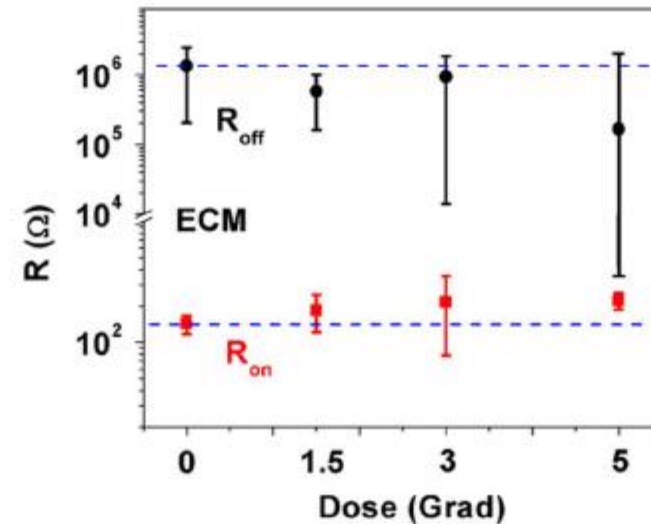
I. Valov and M.N. Kozicki, IEEE Trans. Nucl. Sci, 6, 2862, (2013)

Proton Radiation Hardness Resistive Memories (ReRAMs)

Electrochemical Metallization Memory (EMC)

Pt/HfO(40 nm):Cu/Cu **200 krad/s at a H^+ ion energy of 1 MeV**



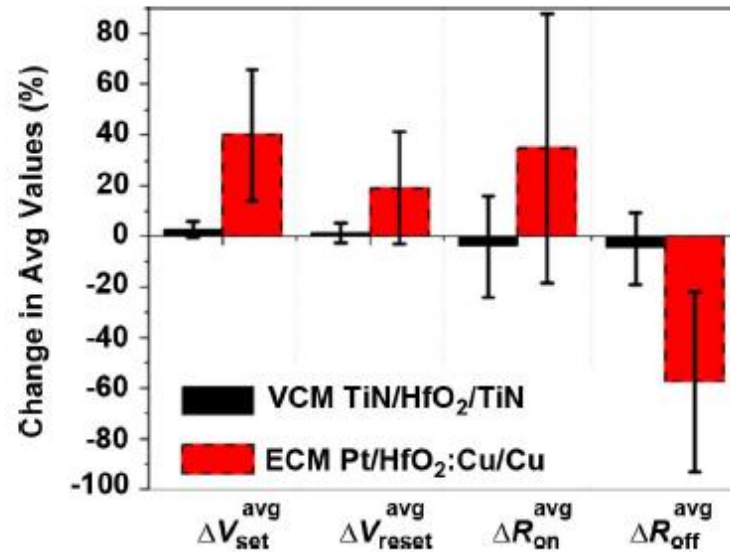


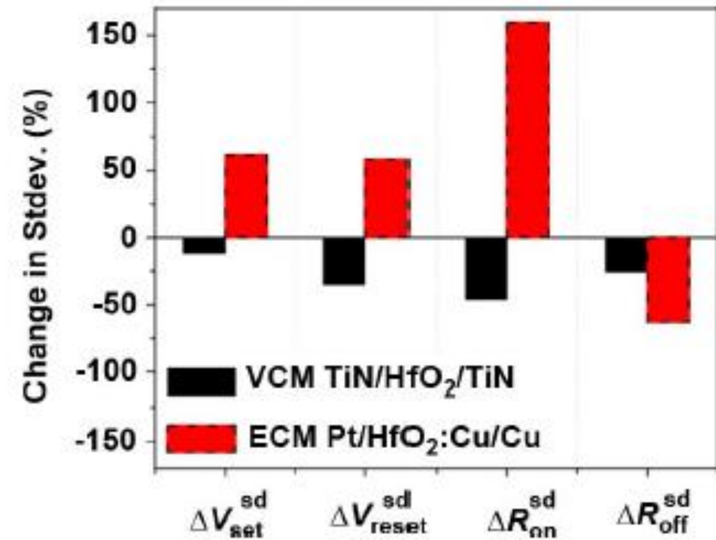
(left) Average V_{set} (in black) and Vreset (in red and (right) average R_{off} (in black) and R_{on} (in red) of all devices at three total doses in ECM ReRAMs. The dashed lines are used as a visual reference to average pre-radiation values

- Radiation increases V_{set} and $|V_{reset}|$
- R_{off} decreases and R_{on} increases slightly for high dose radiation

H. Xiaoli, W. Wei, B, Butcher, S. Tanachutiwat and R.E. Geer, IEEE Trans. Mucl. Sci. 59, 2550 (2012)

Radiation Hardness Resistive Memories (ReRAMs)





Percentage changes and changes in standard deviation after radiation at TID of 1.5 Grad(Si) in average parameters. The values in percentage are all normalized to the pre-radiation values.

- **ECM devices more radiation sensitive than VCM ones**
- **TID Radiation improves uniformity resistive switching in VCM and degrades for ECM**

H. Xiaoli, W. Wei, B, Butcher, S. Tanachutiwat and R.E. Geer, IEEE Trans. Mucl. Sci. 59, 2550 (2012)

Radiation Hardness Resistive Memories (ReRAMs)

- **Overall ReRAMs have a very good radiation hardness**
- **Very high TID doses have to be used to see some effects**
- **Research has to be done to investigate the possible impact of the used materials (e.g. TaO_x, HfO_x, TiO_x, SiO_x) and the technology reproducibility**
- **Pre-radiation variations over the wafer and from wafer to wafer must be taken into account**
- **For metal-doped chalcogenide EMC cells phot doping can occur**
- **Dose rate effects have been observed for very high dose rates**
- **Recent review on state-of-the-art developments:**
  Y. Gonzalez-Velo, H.J Barnaby and M.N Kozicki, Semicond. Sci. Technol. 32, 083002 (2017)

SiGe Devices

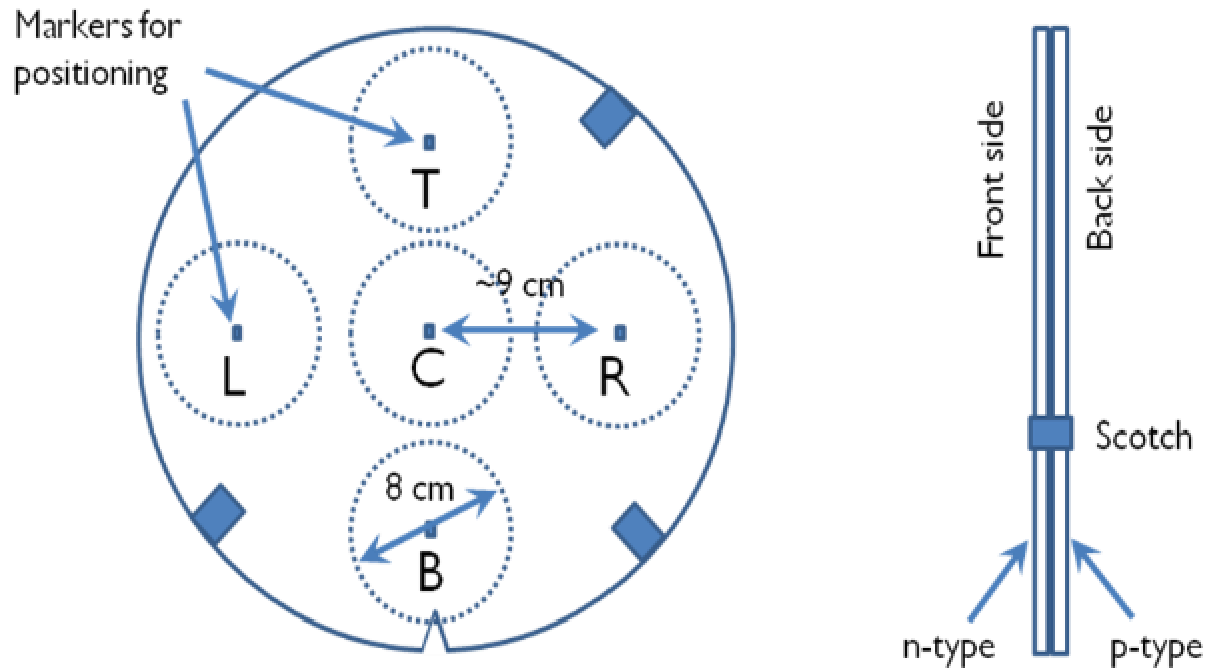
Radiation Conditions

SiGe Technology

60 MeV Proton irradiation on 300 mm wafers

- **Dose rate: $3x10^8$ p/$cm^{-2}s^{-1}$**
- **Total dose: up to $3x10^{12}$ p/cm^2**
- **Louvain-La-Neuve (Belgium)**

Pre-Radiation Wafer Preparation

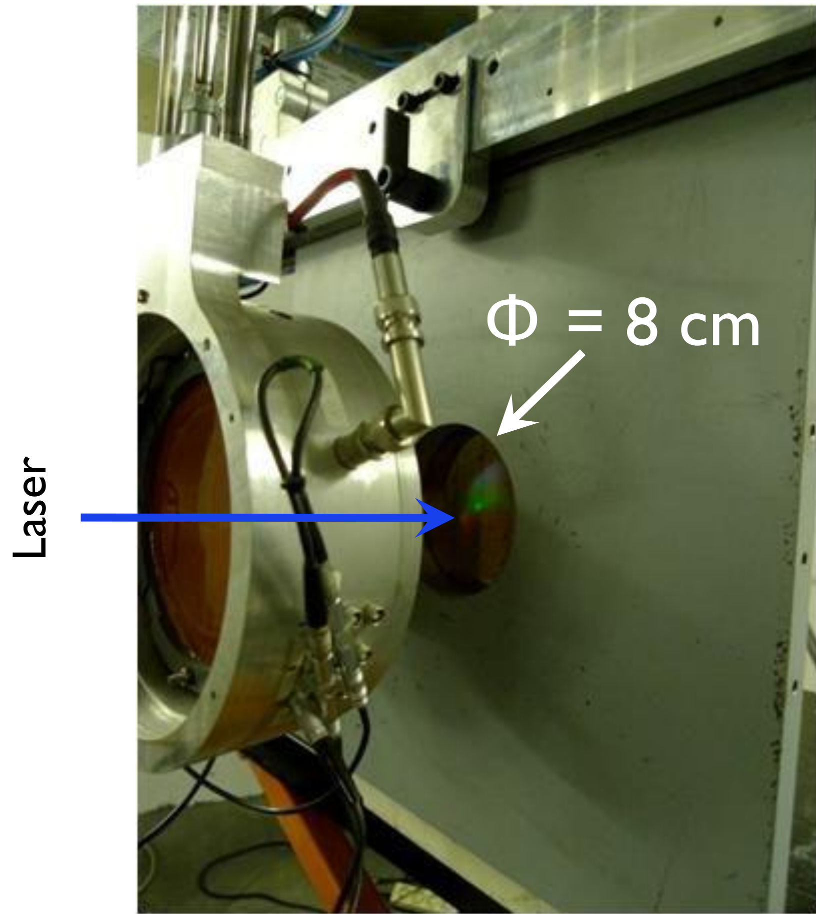


Different wafer zones on the 300 mm wafer (irradiated: L, C and R; references: T and B). Two wafers are fixed together and inserted in the proton-beam setup shown in the right two figures

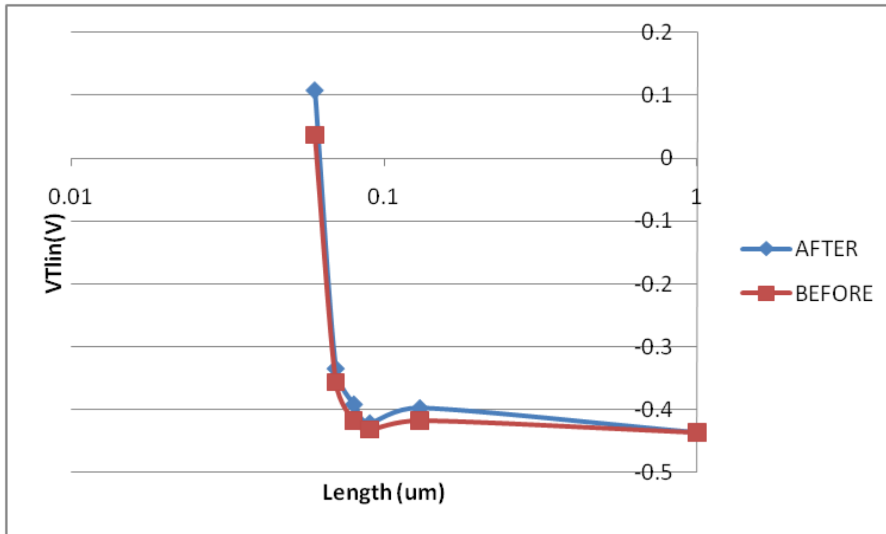
Wafer Setup on Irradiation Apparatus

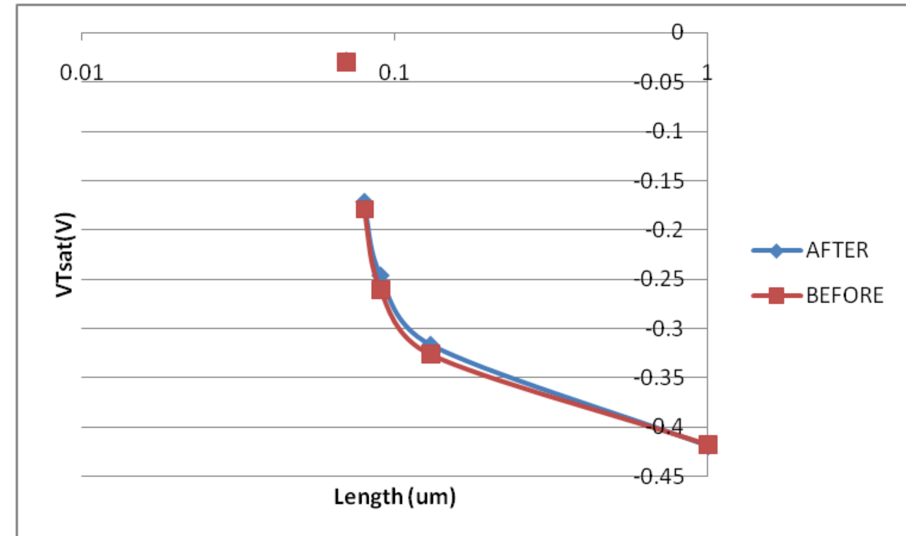
<Front side> **<Back side>**

Laser



Threshold Voltage p-Channel Devices



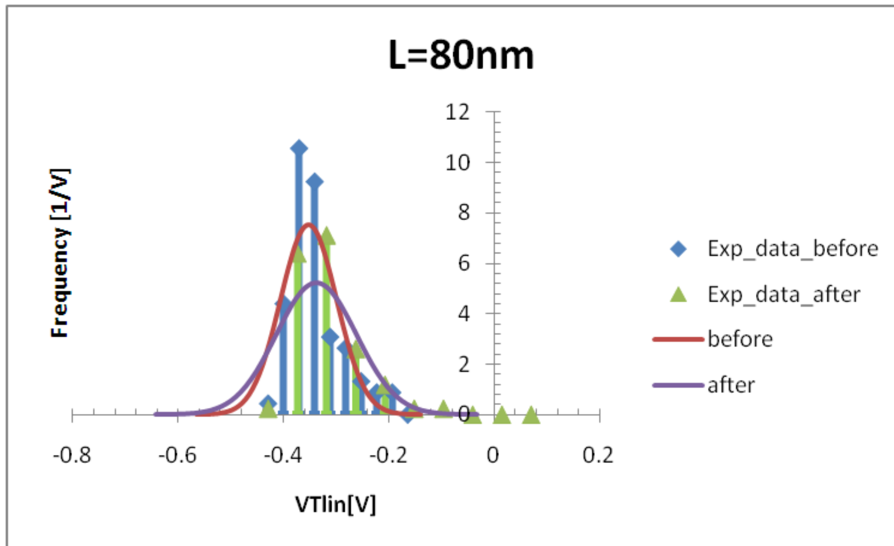


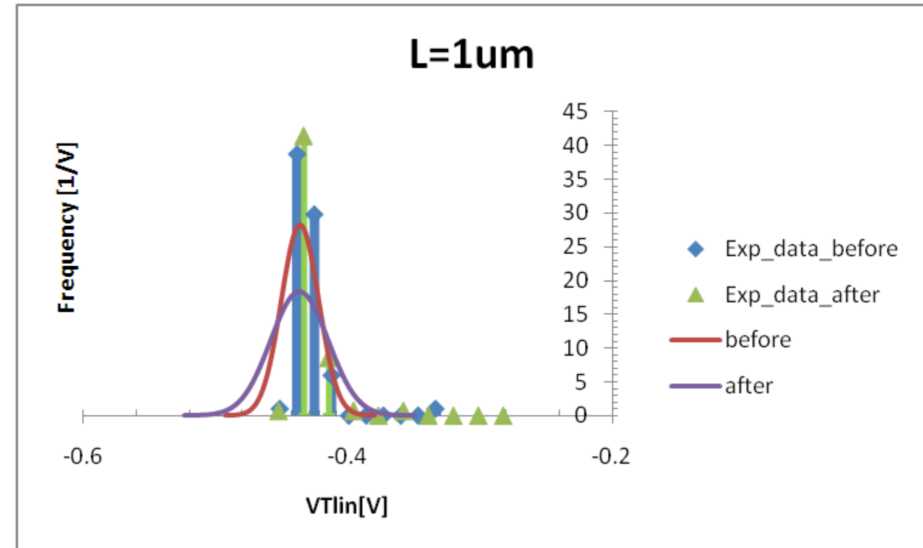
Average values of the pre- and post-irradiation linear threshold voltage at V_{DS}= -50 mV (a) and saturation voltage at V_{DS}= -1 V (b) versus p-channel gate length.

Slightly positive change

Negative charge in oxide or halo de-activation

Statistical p-Channel Threshold Voltage distribution



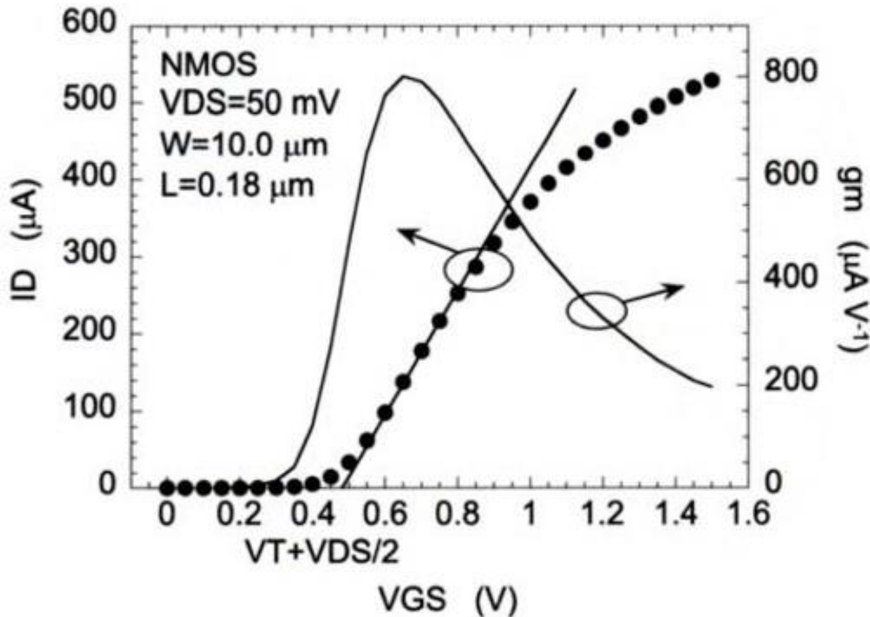


Decrease in V_{Tlin} and wider distribution

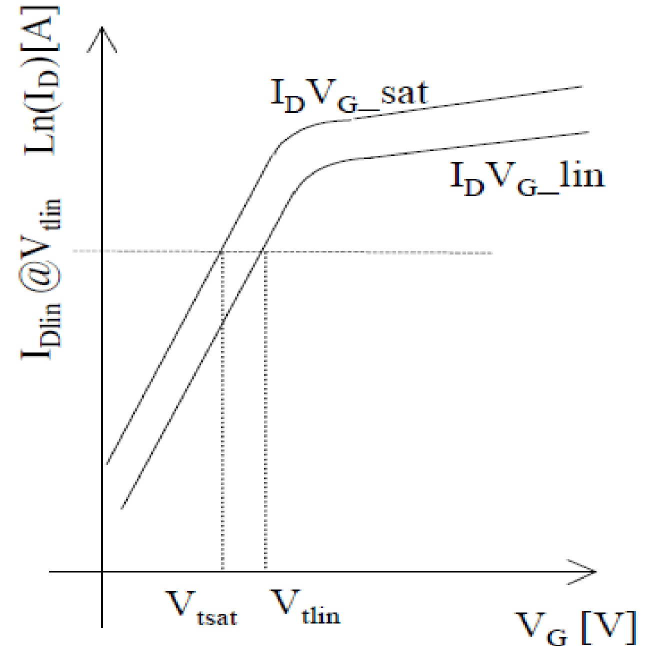
Current in Linear Region and Saturation

$$I_{ds(lin)} = K_0 \times (V_{gs} - V_{Tlin} - \frac{V_{ds}}{2}) \times V_{ds}$$

$$K_0 = \frac{\left\{\frac{\partial I_{ds}}{\partial V_{gs}}\middle| max\right\}}{V_{gs}}$$

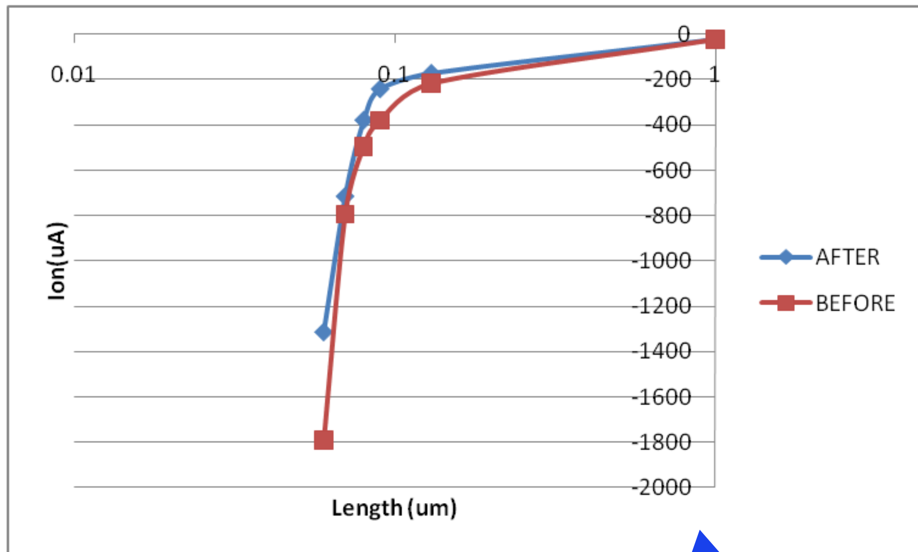


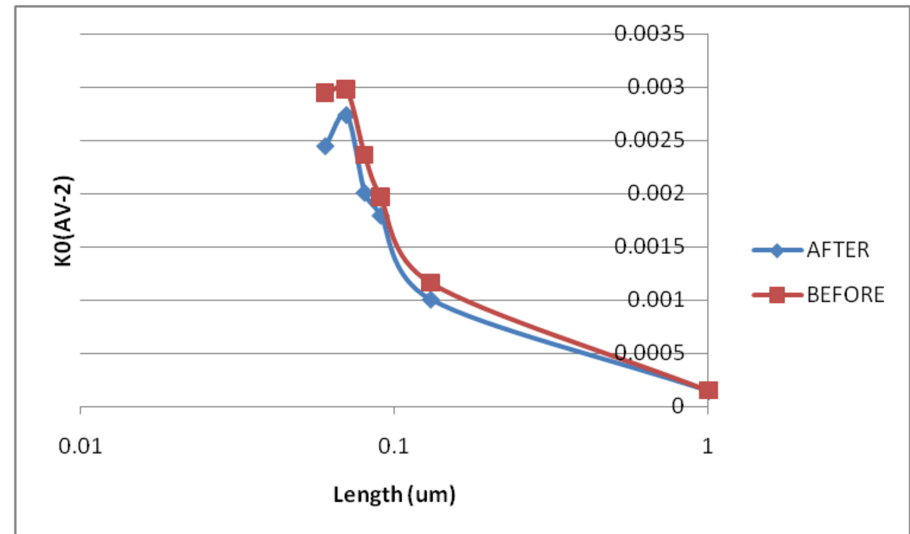
Determination V_{Tlin}



V_{Tsat} (at V_{DS} = 1V) from V_{Tlin}

On-Current and K_0 Factor p-Channel FETs



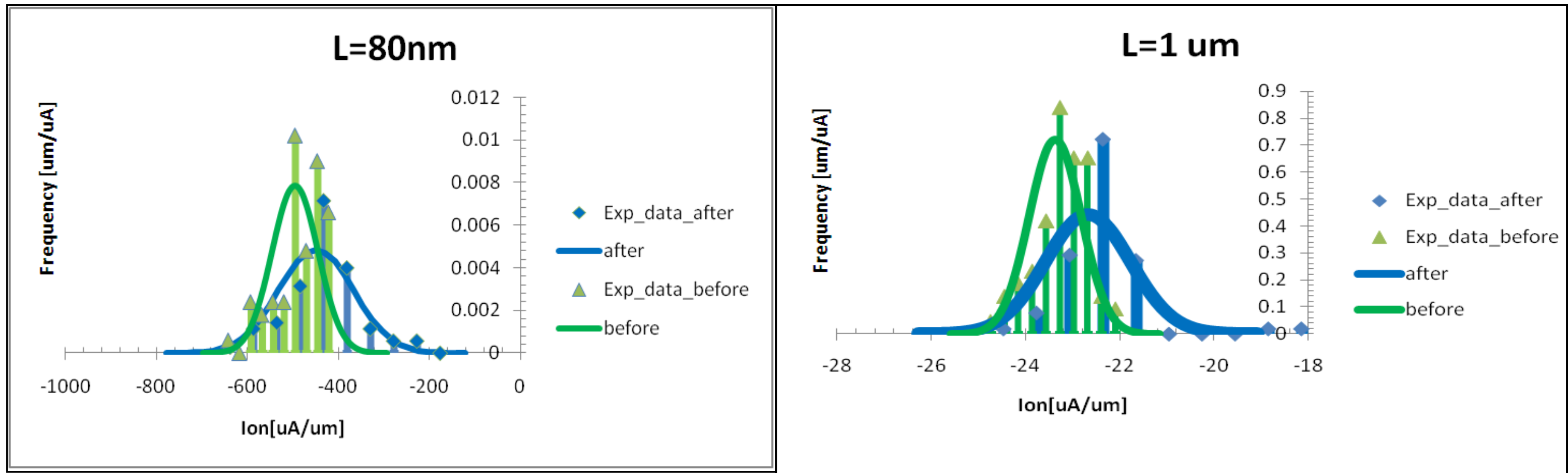


Average values of the pre- and post-irradiation on-current (a) and K_0 value (b) versus p-channel gate length.

Reduction in on-current

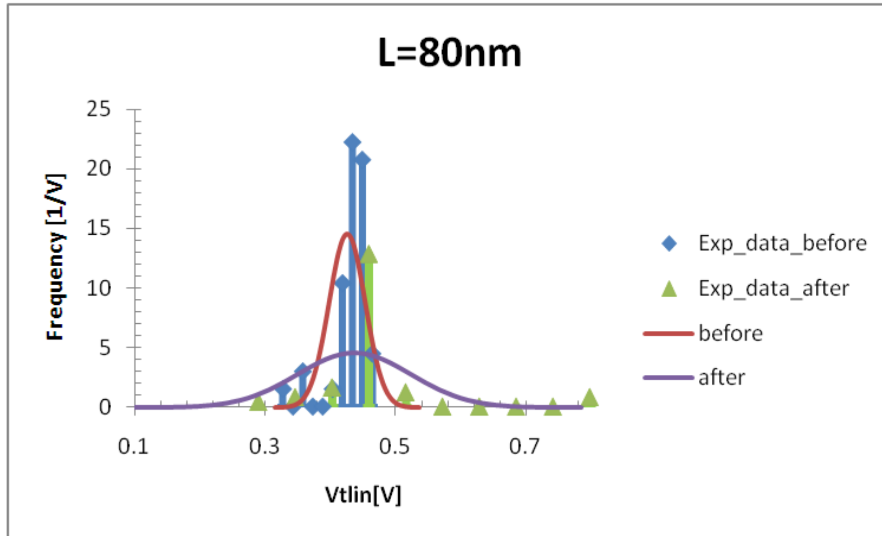
Mobility reduction or series resistance increase

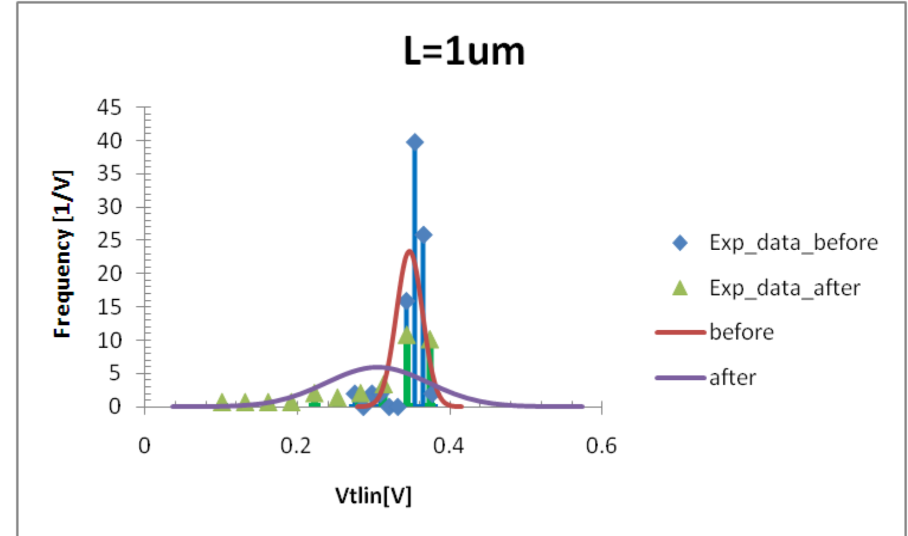
Statistical p-Channel On-Current distribution



- Decrease in I_{on} (25% narrow and 10% longer devices)
- Increase in dispersion

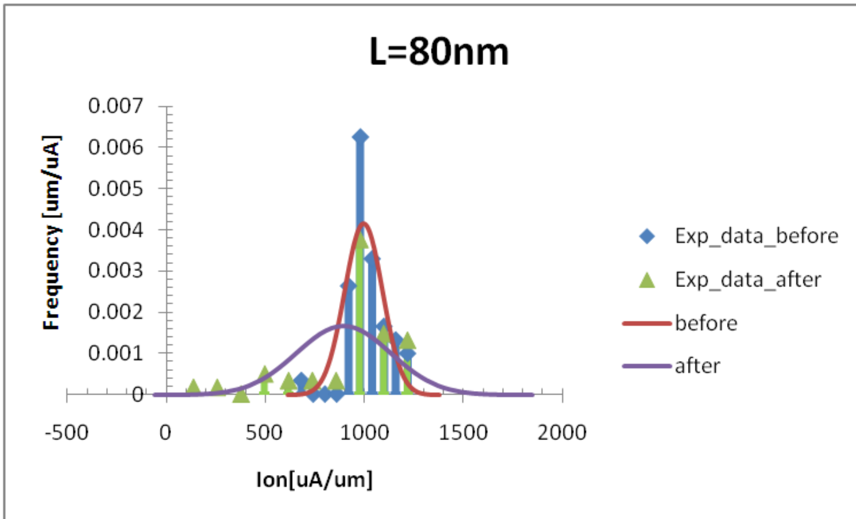
Statistical n-Channel Threshold Voltage distribution

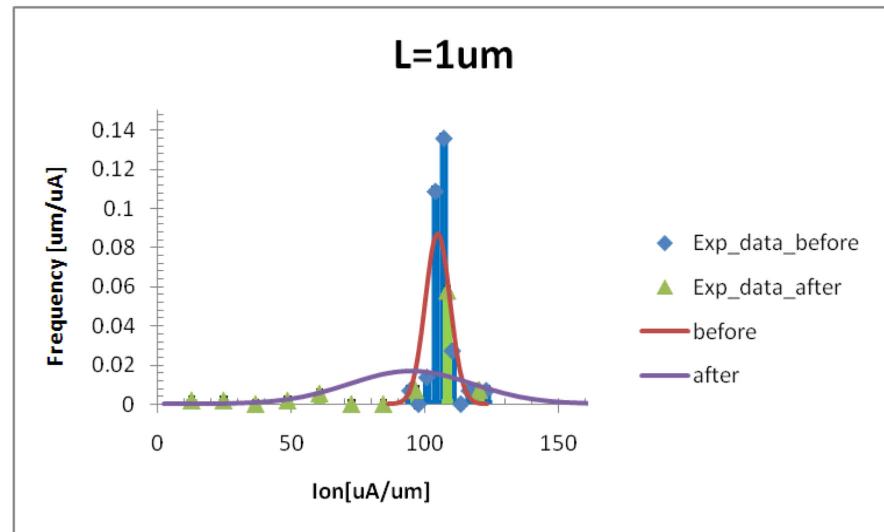




Decrease/Increase in V_{Tlin} for both device lengths wider distribution

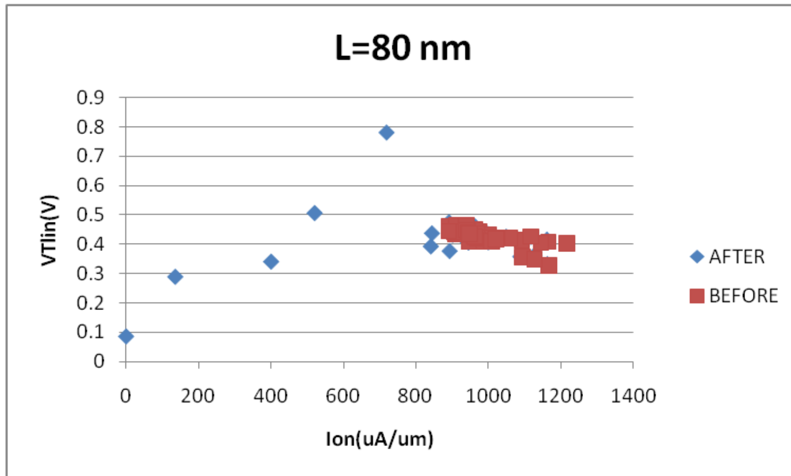
Statistical n-Channel On-Current distribution

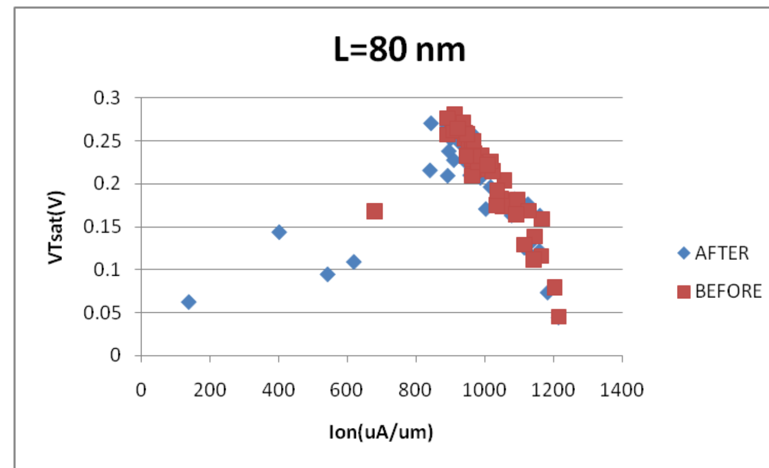


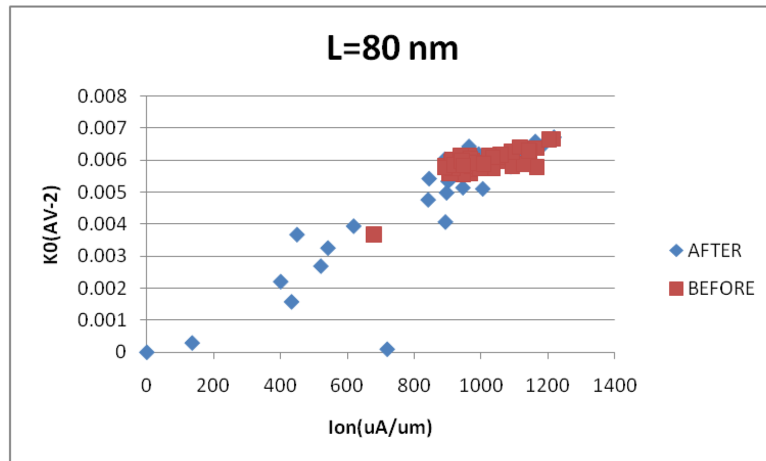


- **Decrease in I_{on} (10% narrow and 12% longer devices) and increase of about 3 in dispersion**
- **Also degradation of the I_{off} observed**

Correlation I_{on} and V_{Tlin}, V_{Tsat} and K_0 for n-Channel

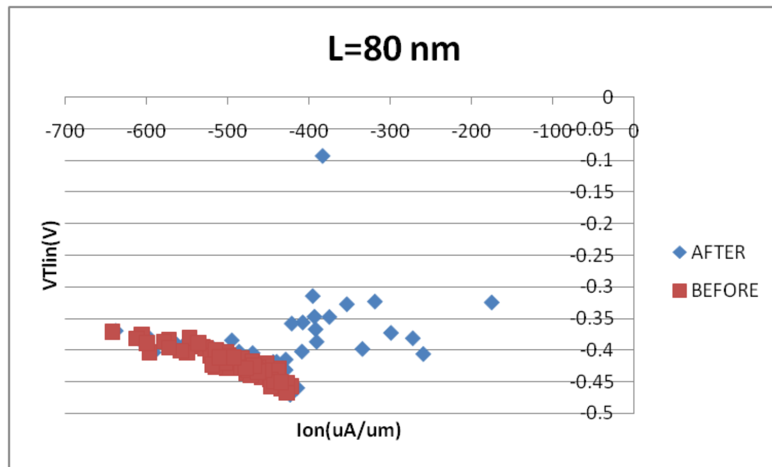


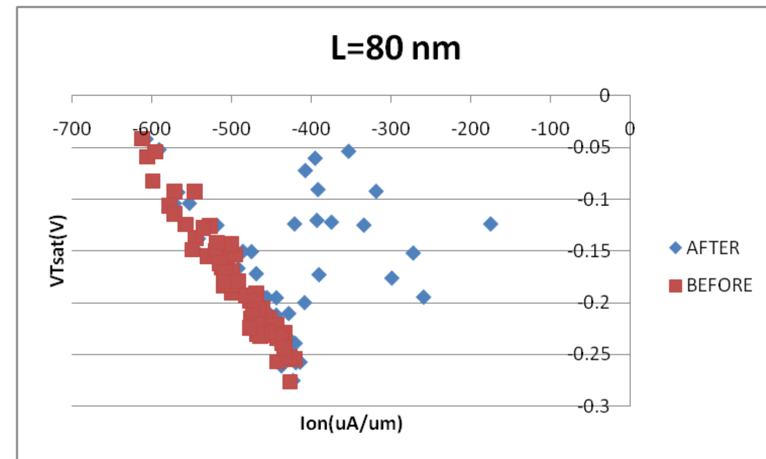


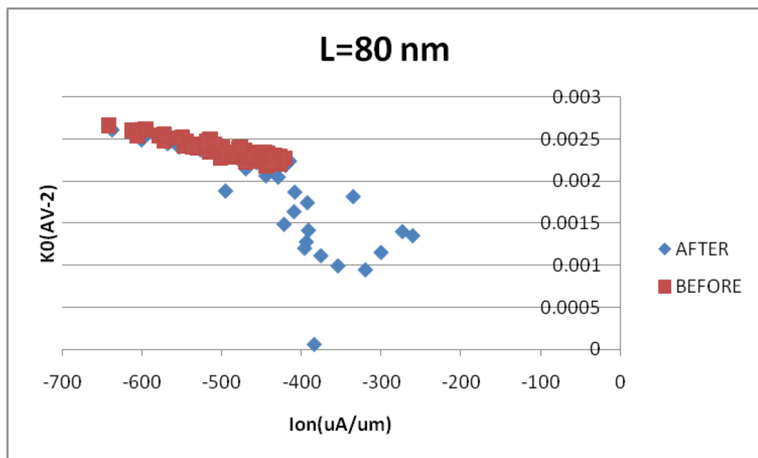


- **Only some correlation for K_0**
- **30% of the devices degraded by the proton irradiation**

Correlation I_{on} and V_{Tlin}, V_{Tsat} and K_0 for p-Channel Devices

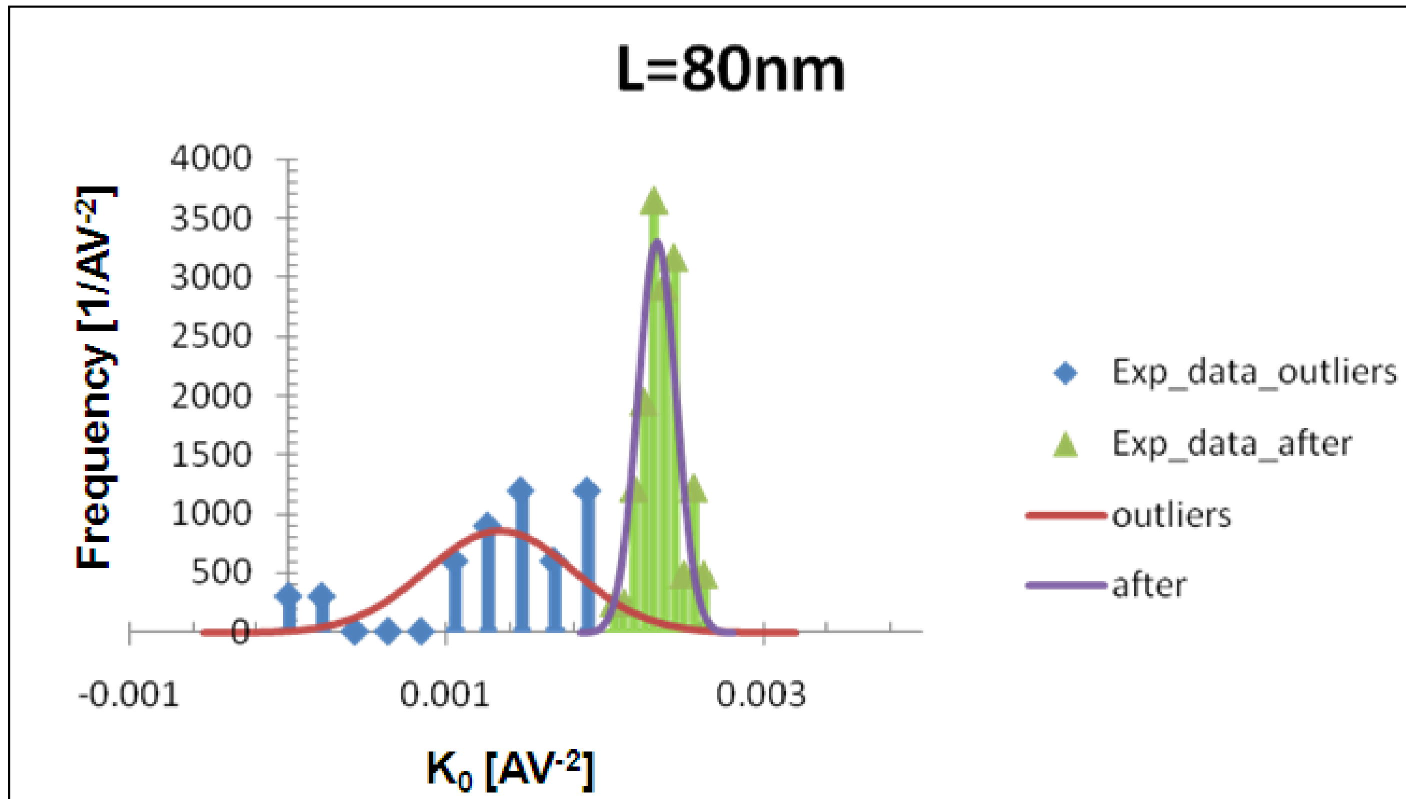






- Some correlation for V_{Tlin} and K_0
- Less for V_{Tsat}
- 20% degraded devices

K_0 Distribution for p-Channel Devices



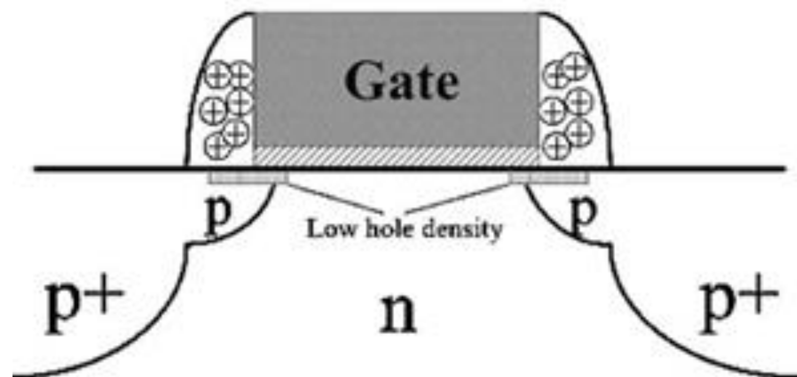
- Distribution functions for both the good devices and the outliers
- The I_{on} degradation correlated with K_0
- Gaussian distribution not the best (bimodal Gaussian)

Radiation Model for p-Channel Devices

Analysis of the outlier devices

On-current degradation only in saturation: ***series resistance***

Trapping in the spacer oxide: impact on LDD region



Radiation Model/2

- Positive shift of the threshold voltage

  Displacement damage impacting the As doping

  Impact of hydrogen – passivation effect?

- No change in subthreshold slope: No interface damage

Radiation Model n-Channel Device

- **Slight increase in subthreshold slope: Interface traps which have an acceptor nature in nMOSFETs (increase V_T)**

  Slight decrease in linear threshold voltage

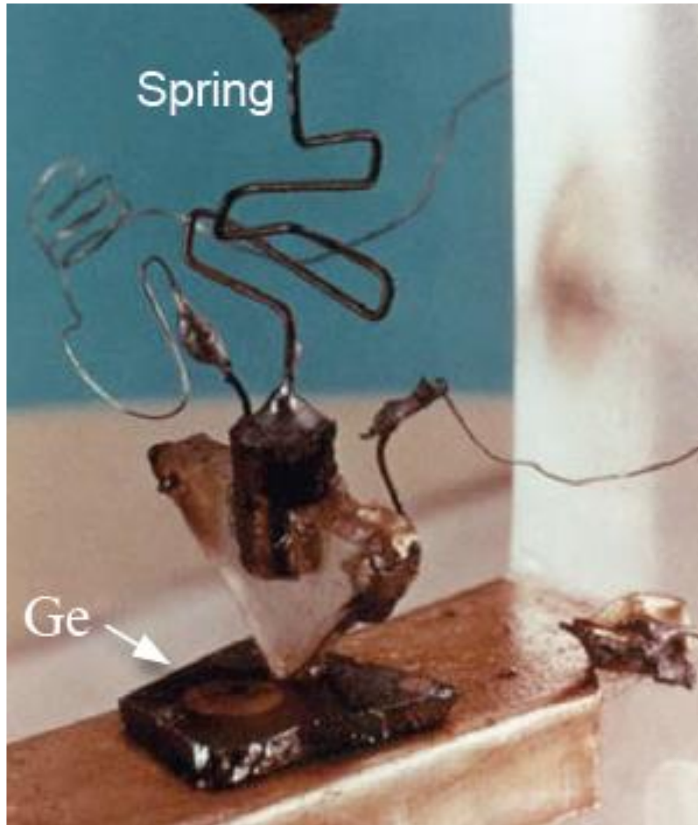
  Strong reduction of the saturation threshold voltage

- **More likely V_T shift caused by positive trapping in the gate dielectric**

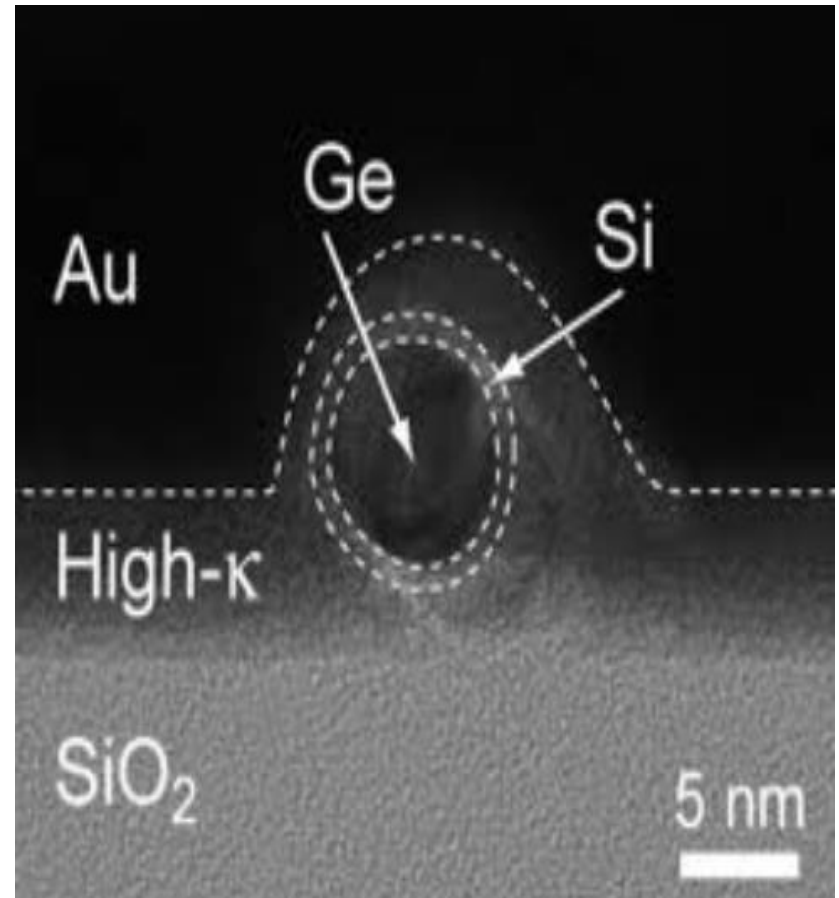
  Influenced by the capping layer used

Ge Devices

Evolution of Ge Devices



1947

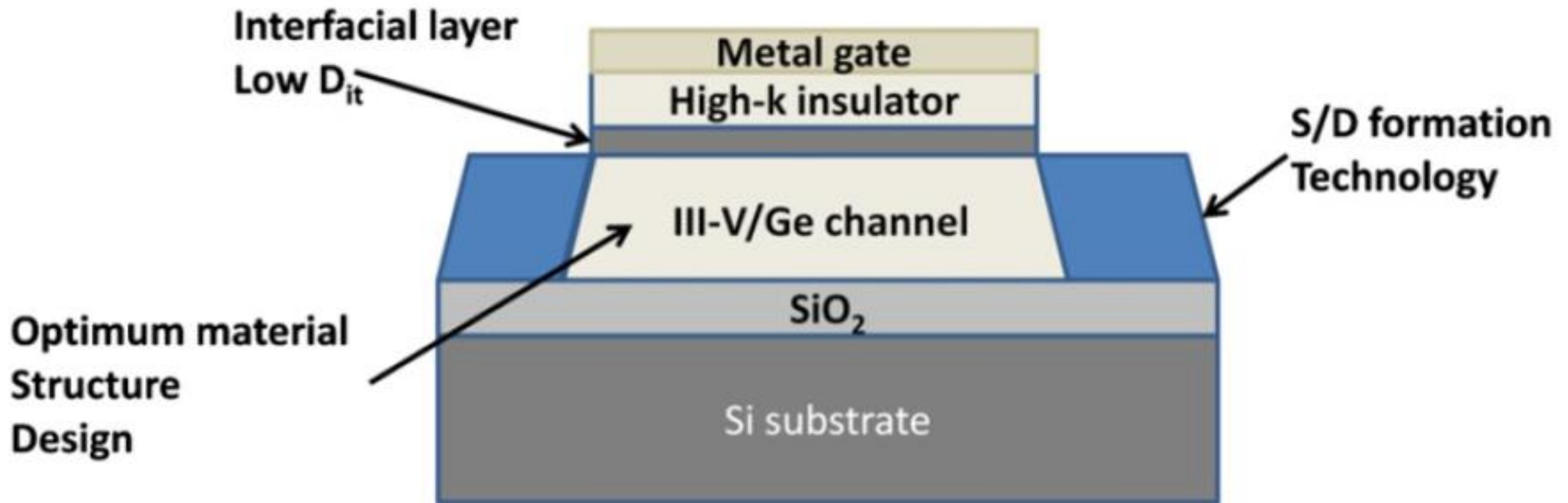


2012

Challenges for Ge MOSFETs

Passivation

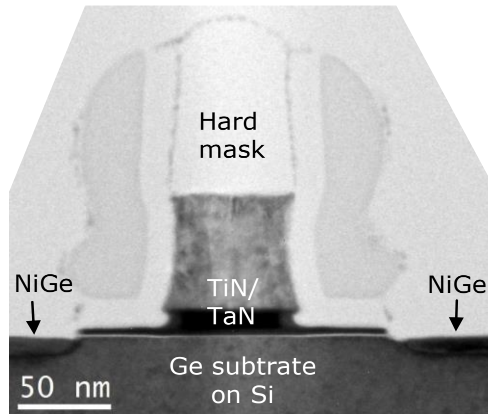
Contact Technology



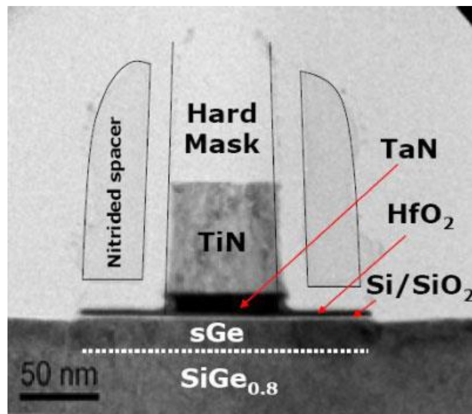
Integration Si platform

Exploration Different Ge Devices

PLANAR

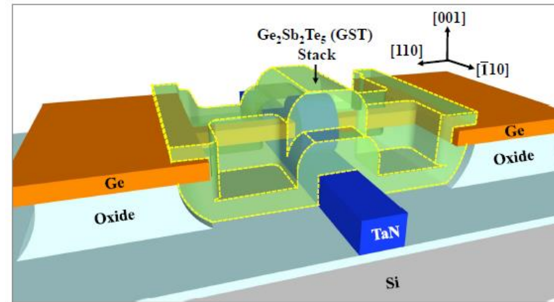


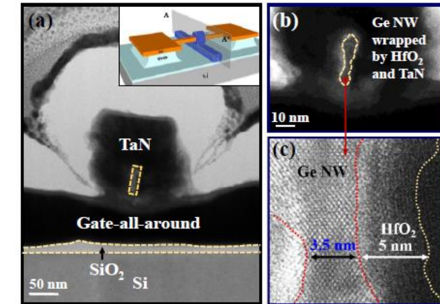
J. Mitard *et al.*, IEDM 2008, p. 873



J. Mitard *et al.*, Jpn. J. Appl. Phys., 50, 04DC17 (2011)

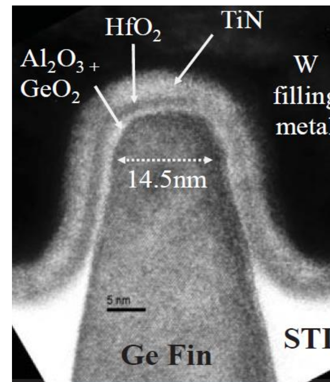
GATE-ALL-AROUND





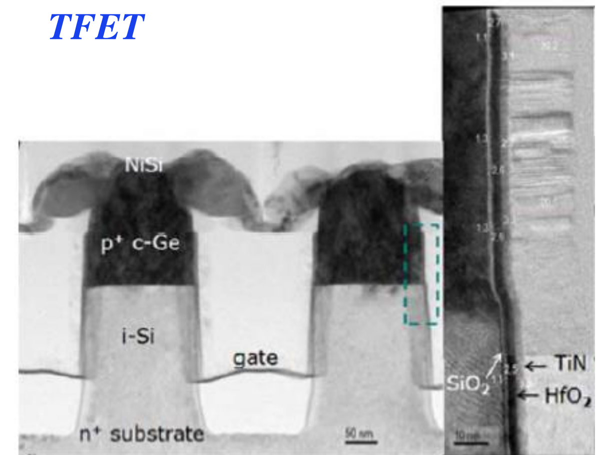
R. Cheng *et al.,* IEDM 2013, 653

FinFET



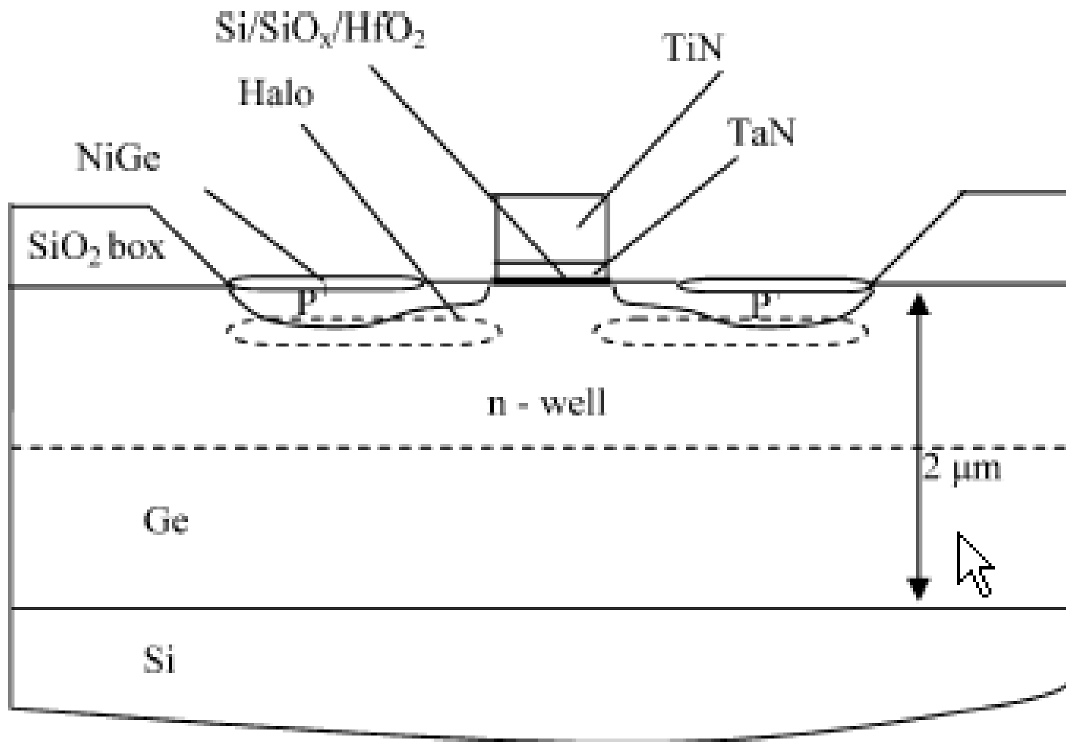
J. Mitard *et al.*, IEDM 2014, 418

TFET



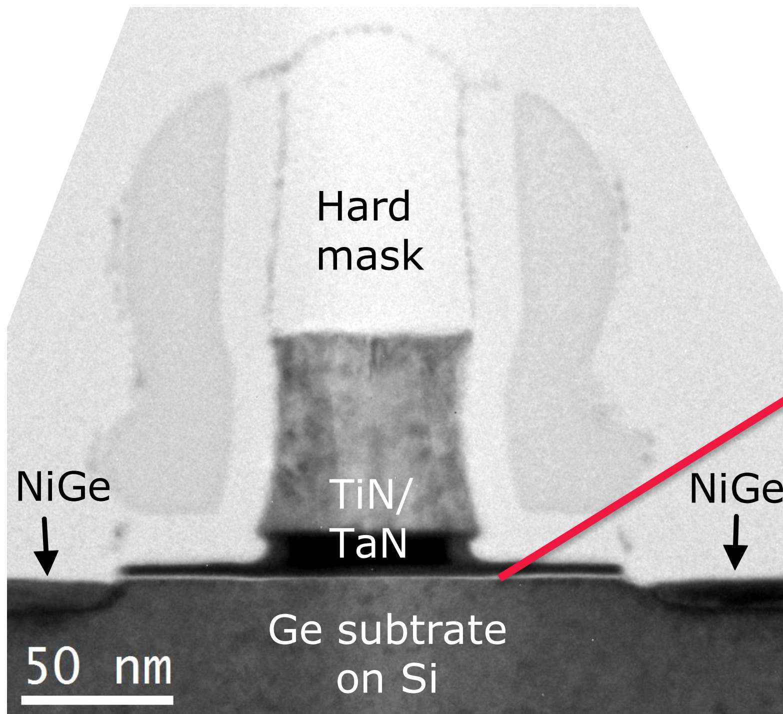
R. Rooyackers *et al.*, IEDM 2013, 92-94

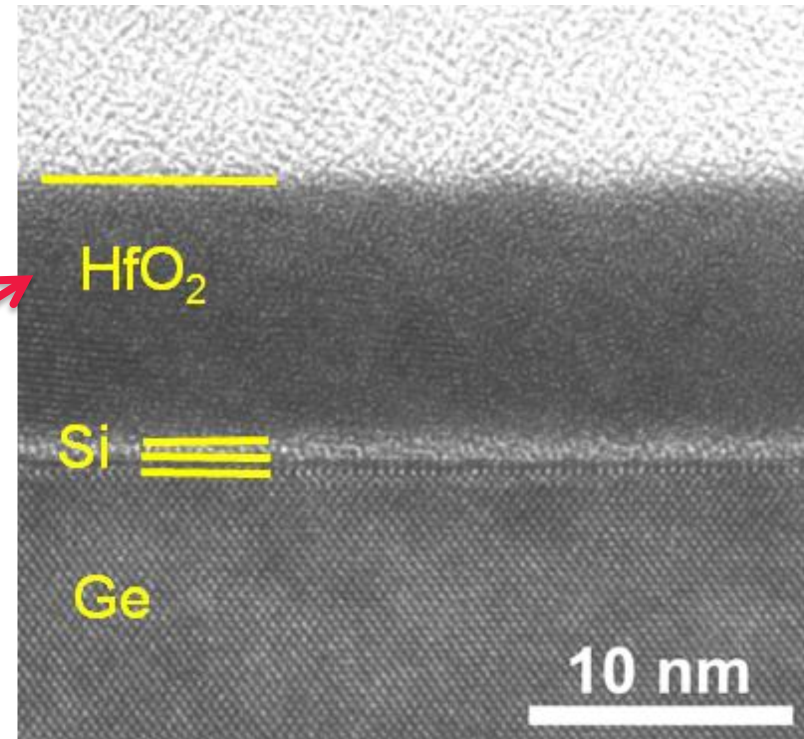
Ge Technology



2 μm Ge (TDD ~ 10^8 cm^{-2})
4 nm HfO_2 (EOT= 1.2 nm)
10 nm TaN/70 nm TiN
550°C JA (x_j = 80 nm)
Ni germanidation

Ge Technology



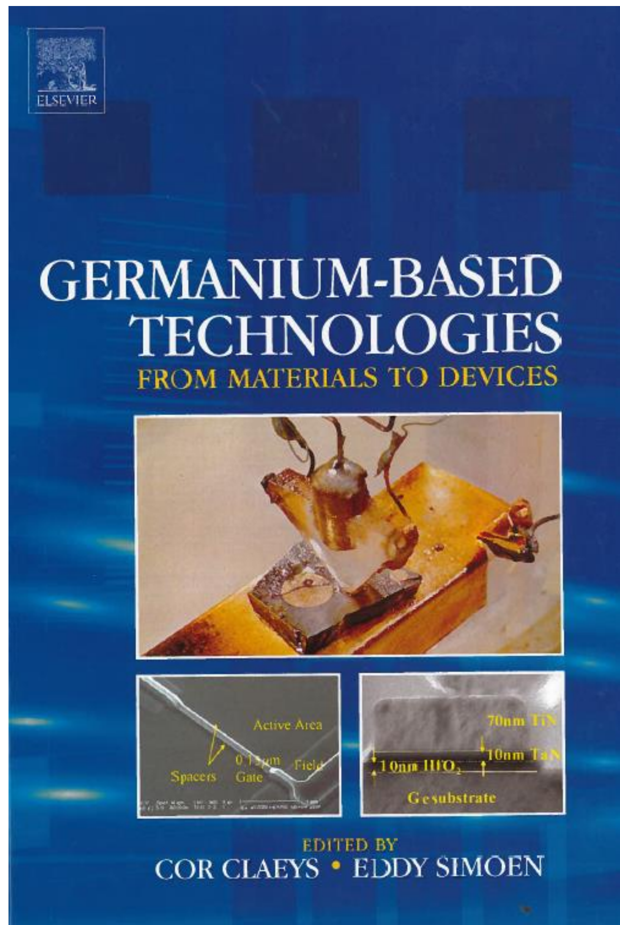


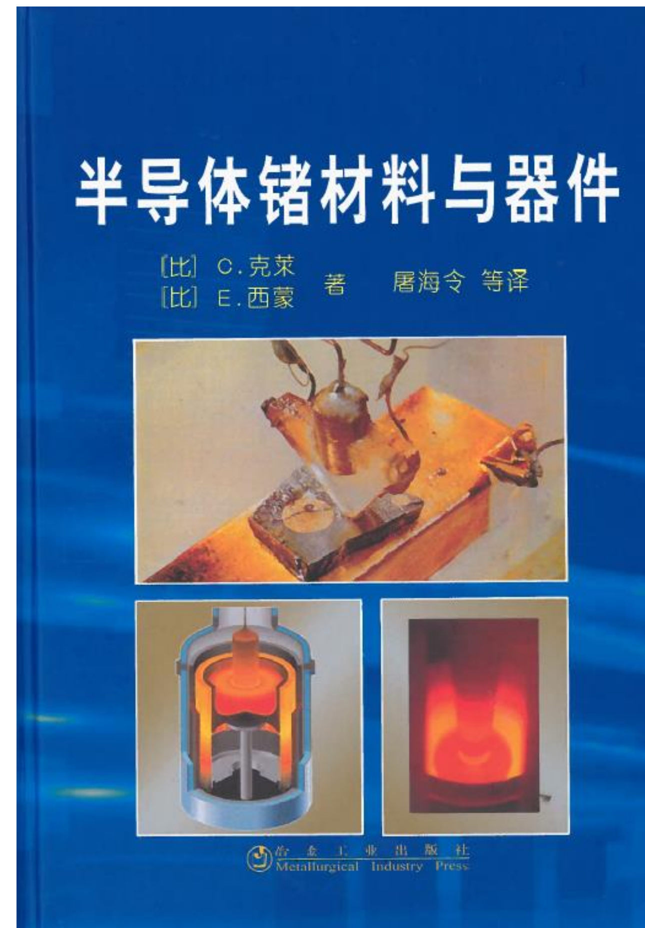
Technological Parameters

- **Epitaxial Si: Thickness (5 or 8 monolayers): Deposition Temperature: 350˚C or 500˚C**
- **Halo implant conditions: As, 80 keV, 3.5, 5 or $6x10^{13}$ cm^{-2}**
- **Extension: B or BF_2**

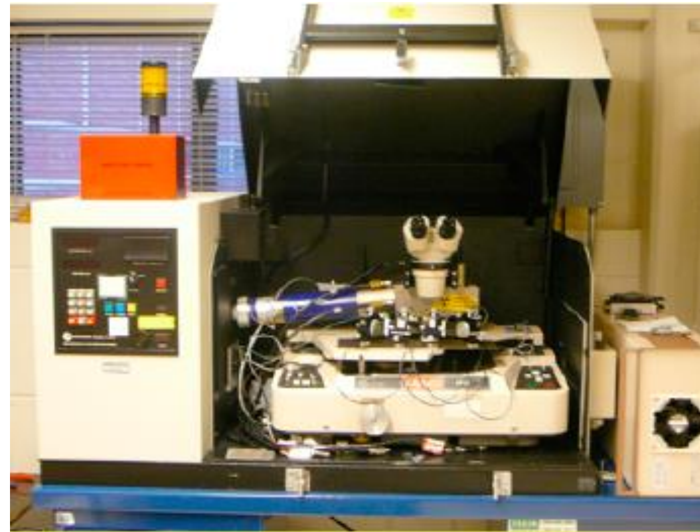
Further Reading

C. Claeys and E. Simoen, "Germanium-Based Technologies: From Materials to Devices", Elsevier, 2007.





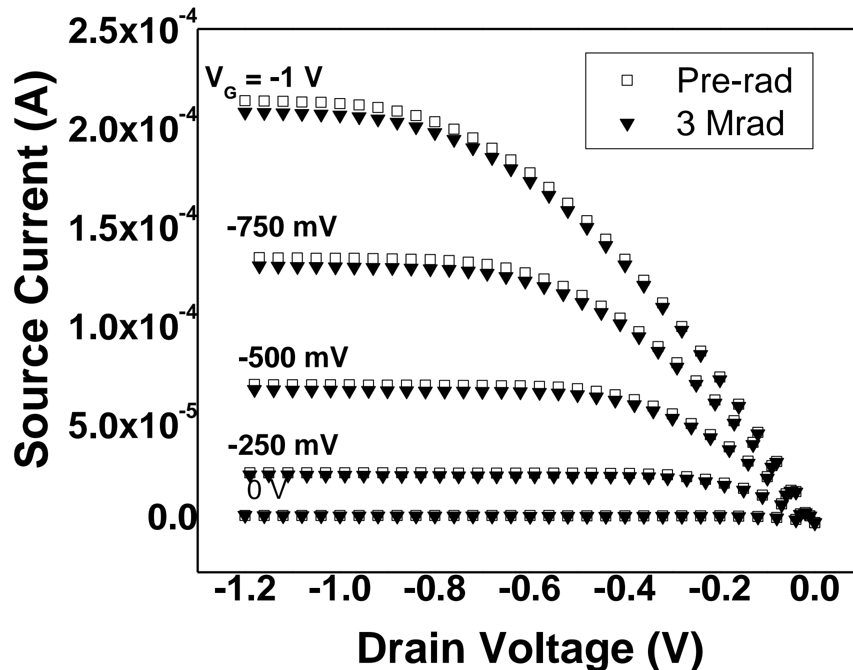
Radiation Conditions

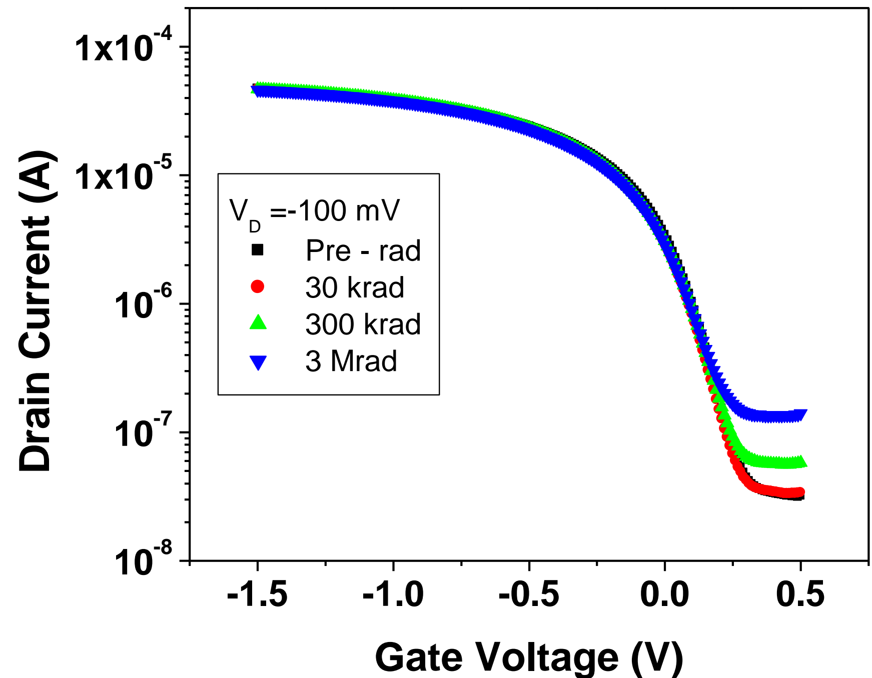


Ge Technology

Wafer level, 10 keV ARACOR x-rays
Gate bias = 1.3 V, other terminals grounded
Cumulative x-ray dose: 3-5 Mrad(SiO_2)
Dose rate: 31.5 krad(SiO_2)/min
Vanderbilt University

Radiation Performance Ge Devices



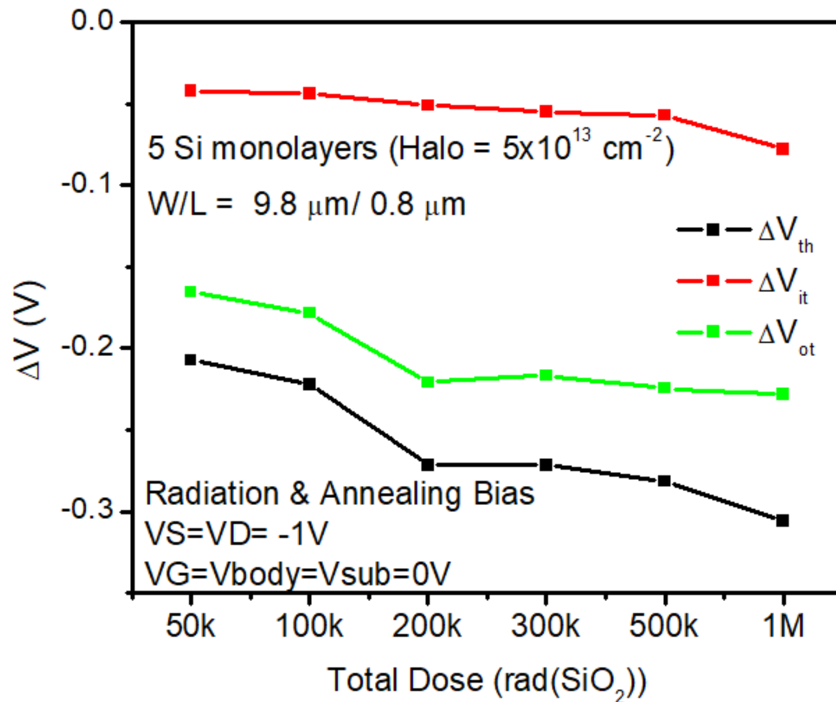


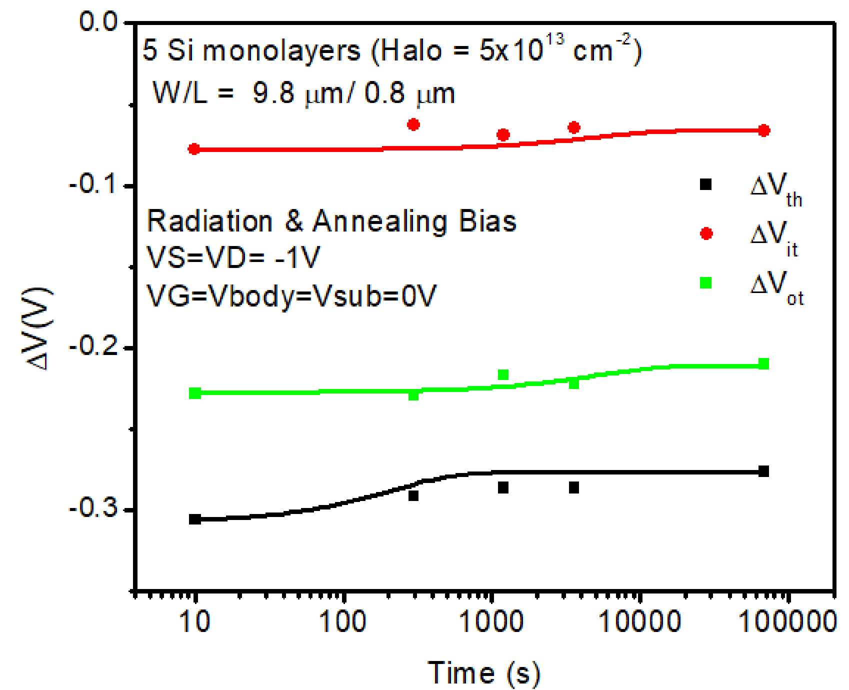
Radiation impact on (a) source current versus drain voltage at different gate voltages and (b) subthreshold drain current vs. gate voltage at V_D= -100 mV for a pMOSFET with W/L = 9.8 µm/10 µm

- **No stretch-out of subthreshold region: Low radiation-induced interface traps**
- **OFF current increases as function of TID**
- **Little change in ON Current**

S.R. Kulkarni, R.D. Schrimpf, K.F. Galloway, R. Arora, C. Claeys and E. Simoen, IEEE Trans. Nucl. Sci., 56, 1926 (2009)

Radiation Performance Ge Devices – Threshold Voltage

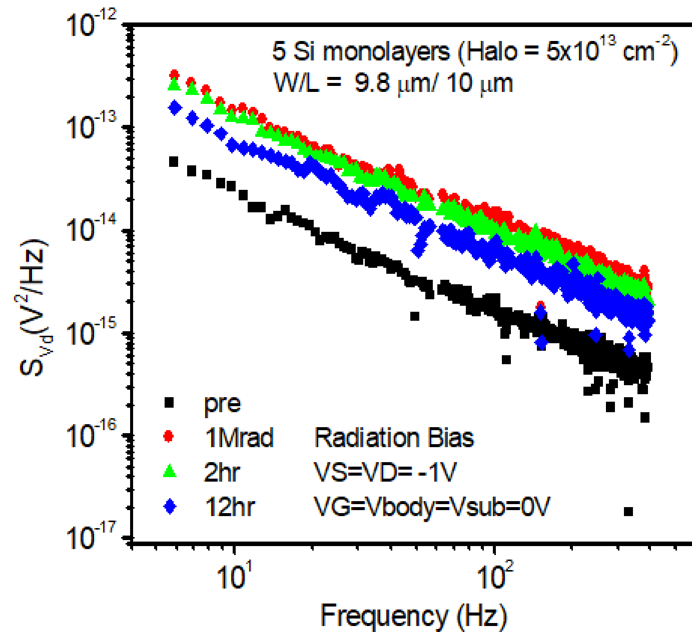


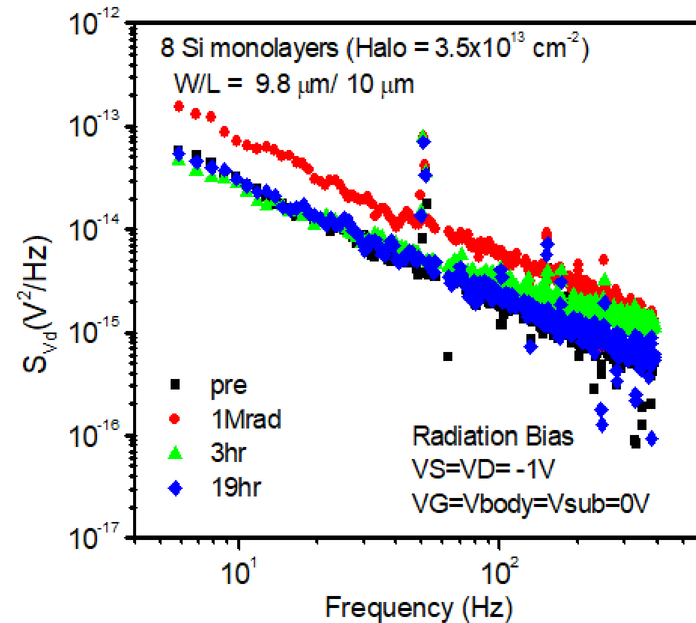


Threshold voltage shift ΔV_{th}, interface trap charge voltage shift ΔV_{it}, and oxide trap charge voltage shift ΔV_{ot} (a) as a function of irradiation and (b) as a function of isothermal annealing time at room temperature. All devices have W/L = 9.8 µm/0.8 µm.

C. X. Zhang, S. A. Francis, E. X. Zhang, D. M. Fleetwood, R. D. Schrimpf, K. F. Galloway, E. Simoen, J. Mitard and C. Claeys, RADCES 2010

Radiation Performance Ge Devices – Noise Behavior



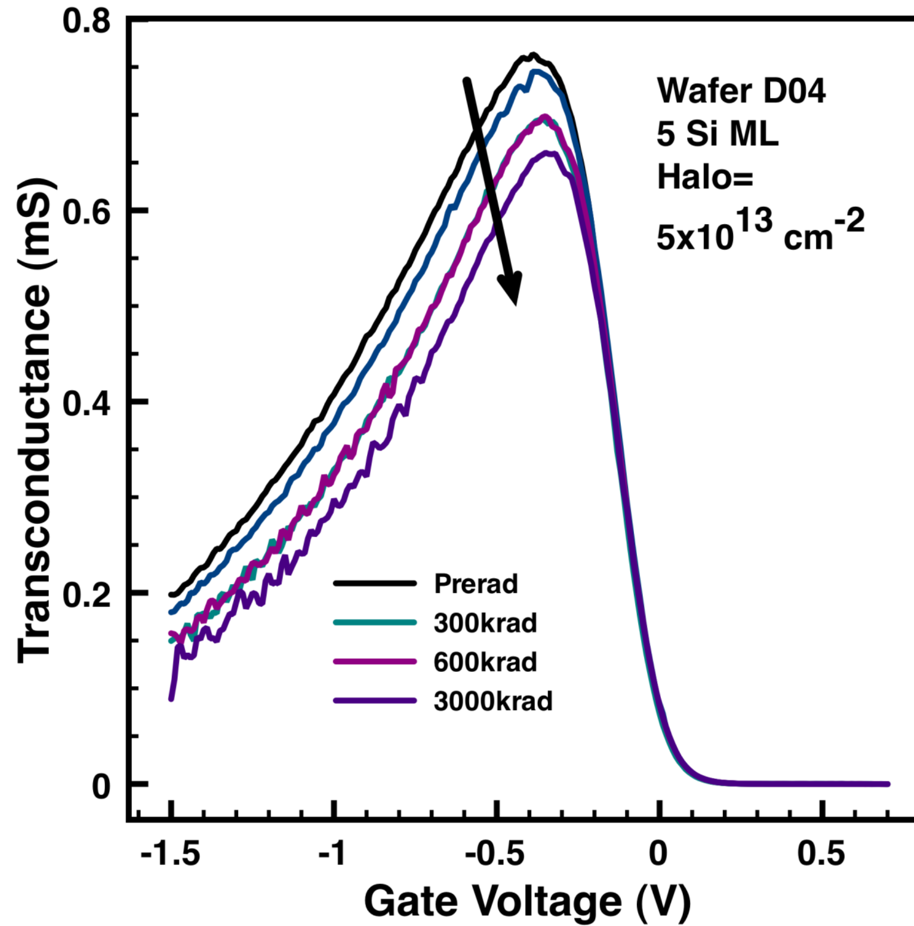


Excess drain-voltage noise power spectral density S_{Vd} as a function of frequency for (a) Ge pMOS transistors with 5 Si monolayers and *W/L*= 9.8 µm/10 µm, and (b) Ge pMOS devices from another wafer in the same process lot, which had 8 Si monolayers. Impact of room temperature annealing.

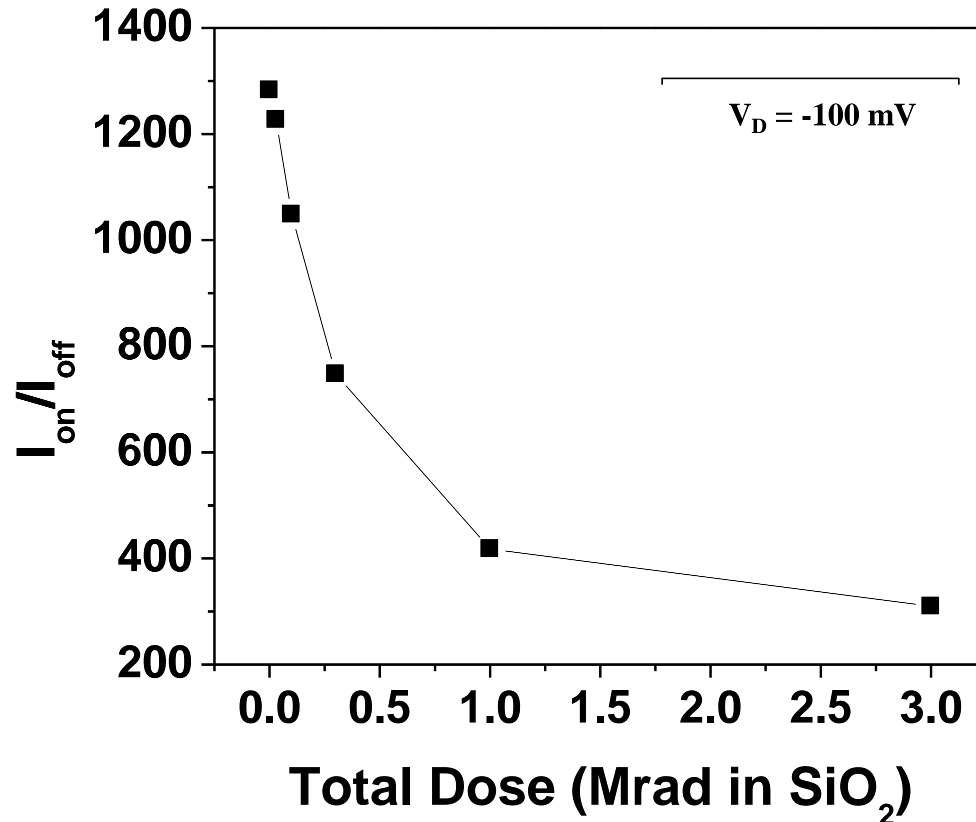
The increase in noise is lower for a thicker Si monolayer and the annealing is more complete

C. X. Zhang, S. A. Francis, E. X. Zhang, D. M. Fleetwood, R. D. Schrimpf, K. F. Galloway, E. Simoen, J. Mitard and C. Claeys, RADCES 2010

Radiation Performance Ge Devices



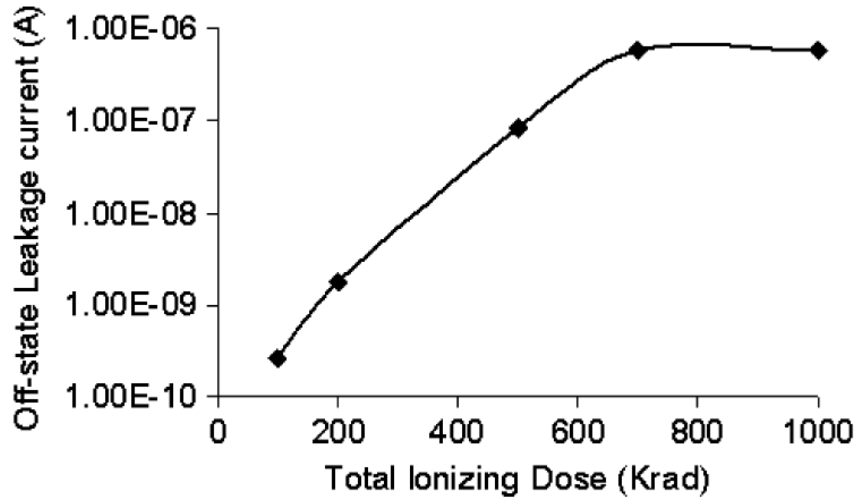
Radiation Performance Ge Devices



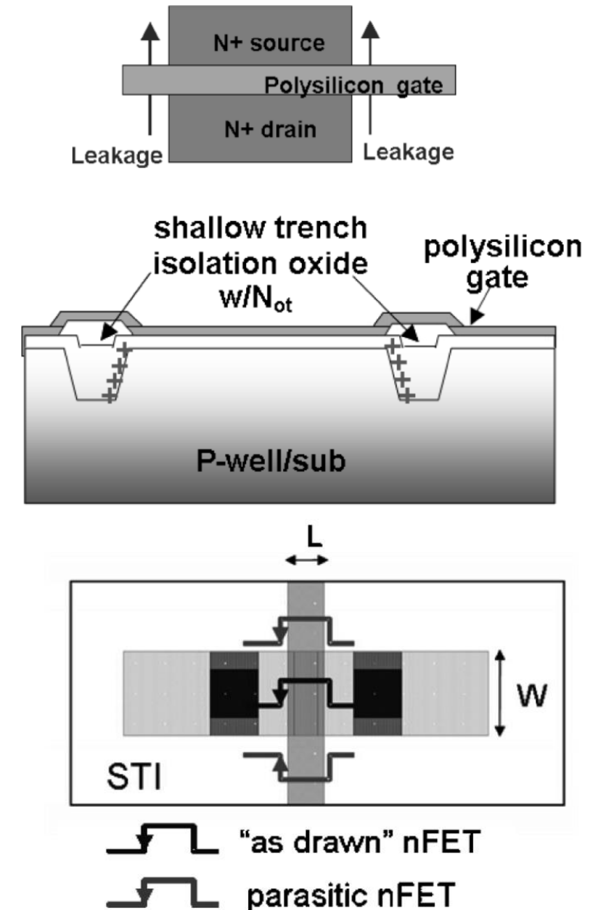
Increase in the off-state current is related to leakage current between the reverse-biased drain and the substrate. For Si this due to charge trapped in the isolation oxide (Si/SiO_2 sidewall of the trench).

S.R. Kulkarni, R.D. Schrimpf, K.F. Galloway, R. Arora, C. Claeys and E. Simoen, IEEE Trans. Nucl. Sci., 56, 1926 (2009)

Radiation Performance Si Devices



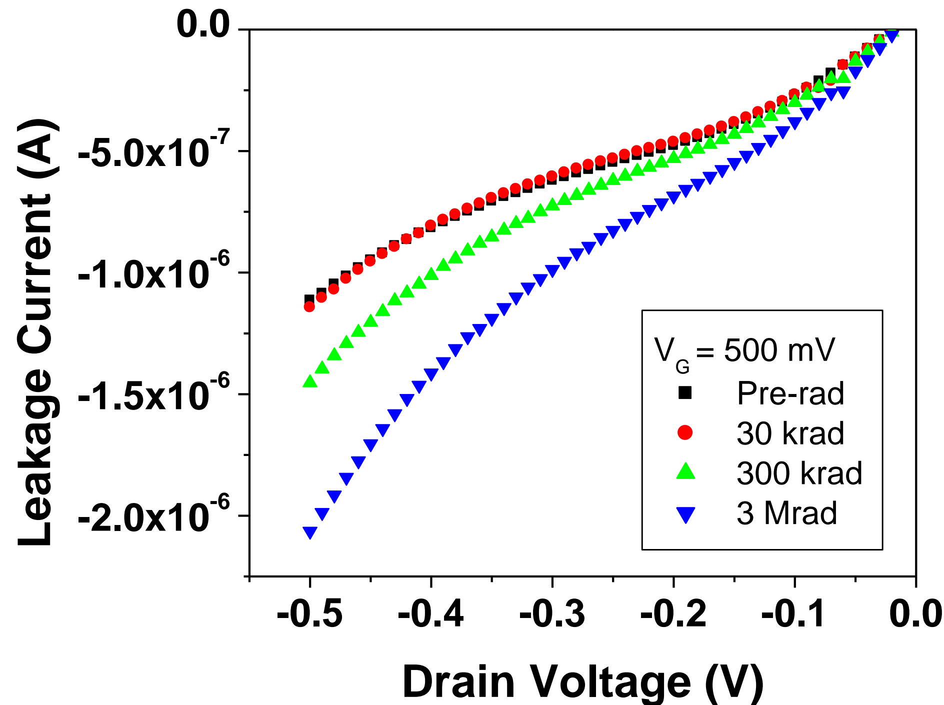
Off-state leakage as a function of TID. Saturation of I_{off} for TID > 600 Krad at a leakage current in the order of 10^{-7} A.



Increase in the off-state current is due to charge trapped in the isolation oxide (Si/SiO_2 sidewall of the trench)

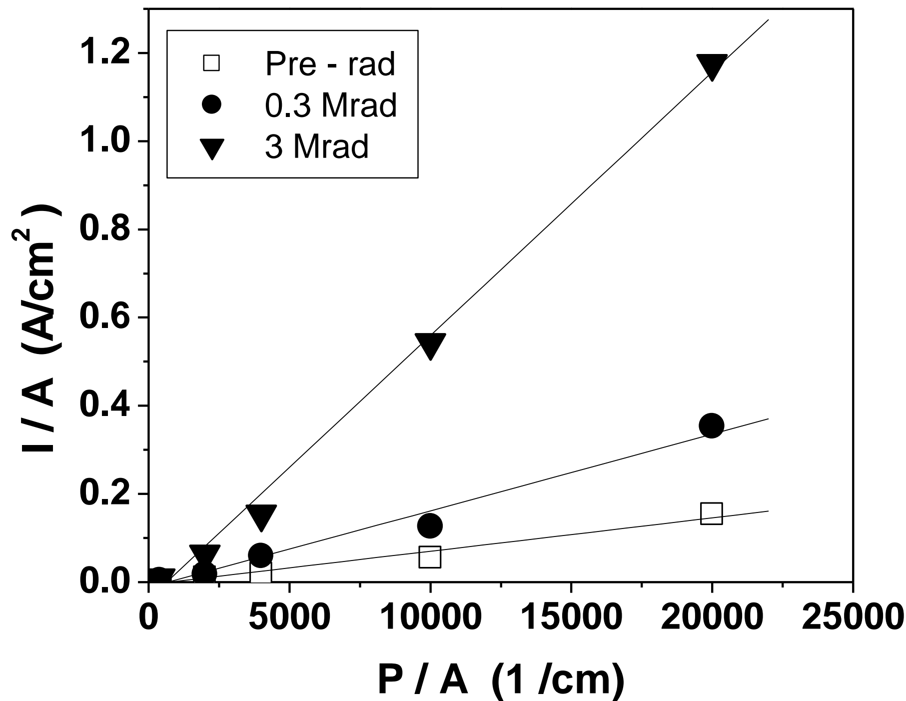
I.S. Esqueda, H.J. Barnaby and M.L. Alles, IEEE Trans. Nucl. Sci., 52, 2259 (2005)

Cause for Wafer Leakage



$$J = J_{diffusion} + J_{generation} + J_{surface\ generation}$$

Current Density vs Perimeter/Area



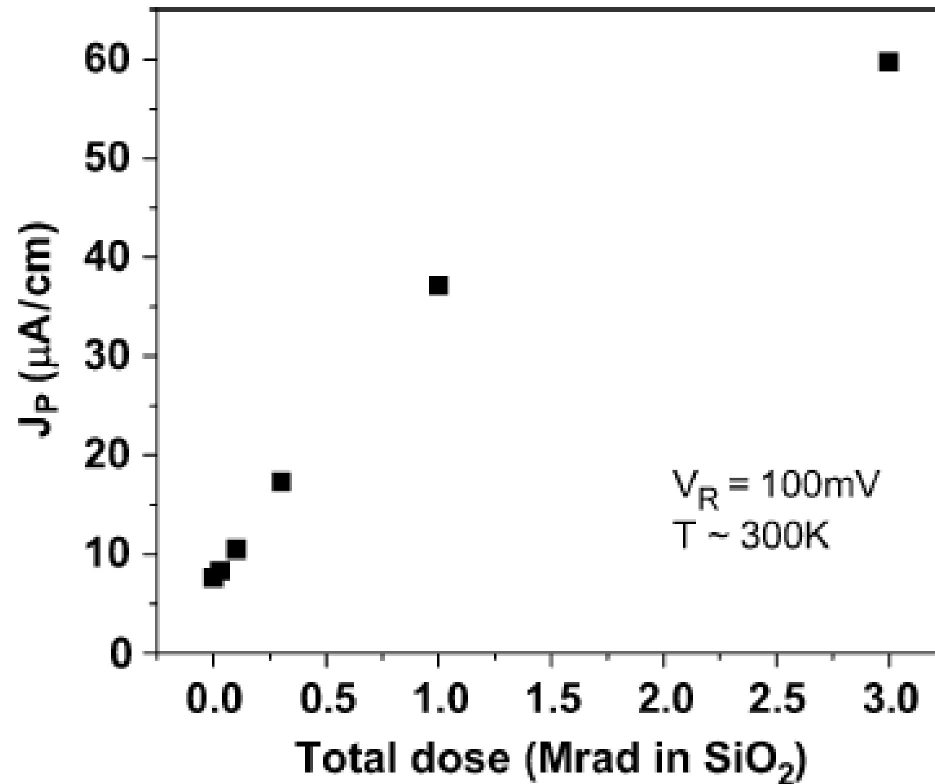
$$J_A + J_P\,(P/A) = I/A$$

J_A: Area current density
J_P: Perimeter current density

Slope change (intercept constant) implies surface generation dominates

S.R. Kulkarni, R.D. Schrimpf, K.F. Galloway, R. Arora, C. Claeys and E. Simoen, IEEE Trans. Nucl. Sci., 56, 1926 (2009)

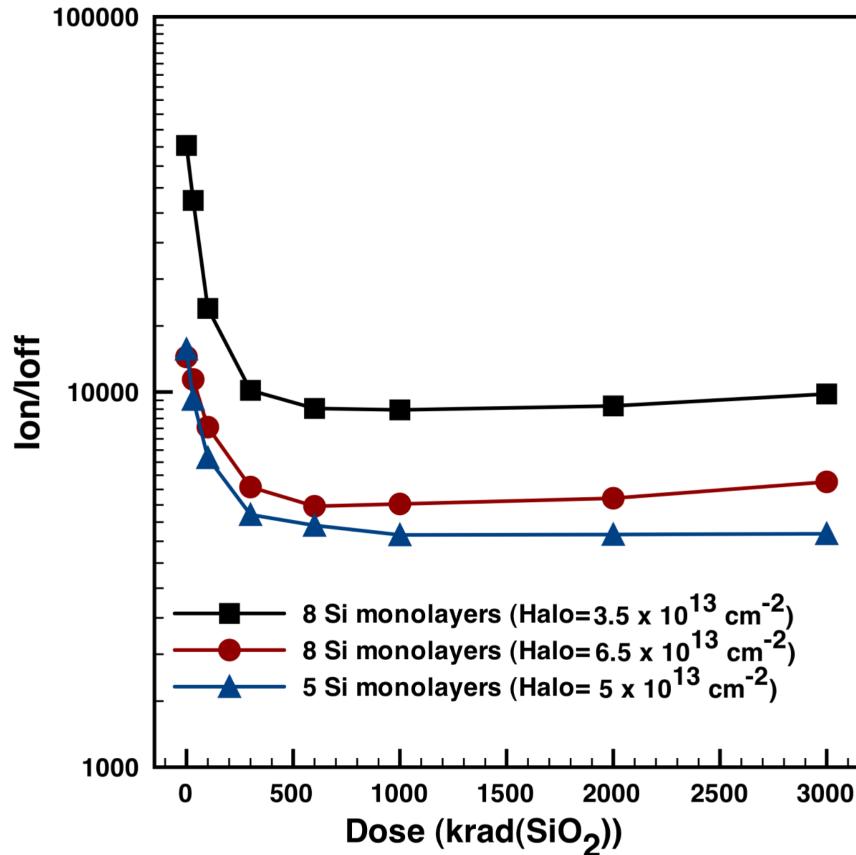
Perimeter Current Density vs Dose



Peripheral current density as a function of dose for a set of diodes with different geometries

S.R. Kulkarni, R.D. Schrimpf, K.F. Galloway, R. Arora, C. Claeys and E. Simoen, IEEE Trans. Nucl. Sci., 56, 1926 (2009)

Radiation Performance Ge Devices

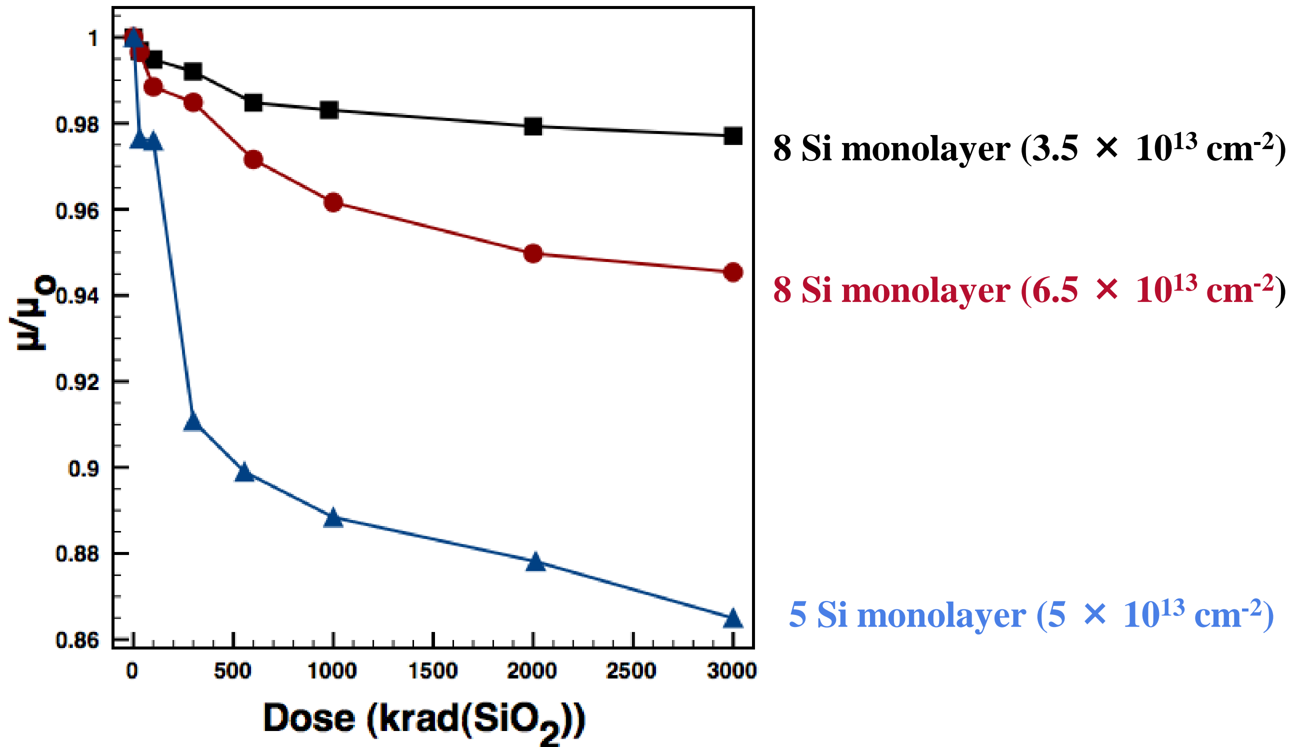


- Highest starting ratio for 8 Si ML and low halo dose
- For 5 Si ML a faster fall off behavior

Influence of the halo dose and the thickness of the Si capping layer as a function of total dose for a pMOSFET with W/L = 9.8 µm/10 µm .

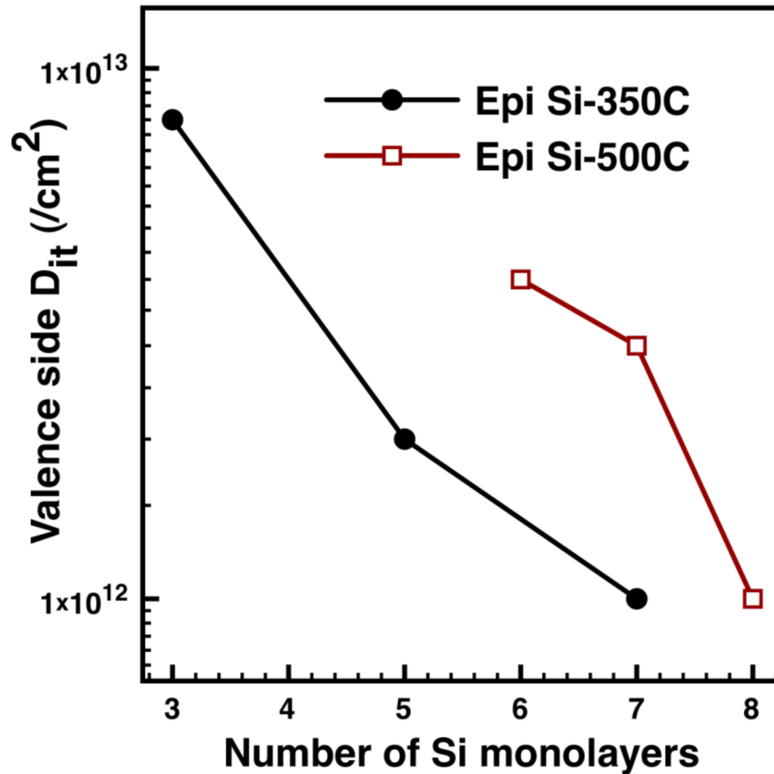
R. Arora, E. Simoen, E.X. Zhang, D.M. Fleetwood, R.D. Schrimpf, K.F. Galloway, B.K. Choi, J. Mitard, M. Meuris, C. Claeys, A. Madan and J.D. Cressler, IEEE Trans. Nucl. Sci., 57, 1933 (2010)

Mobility Comparison



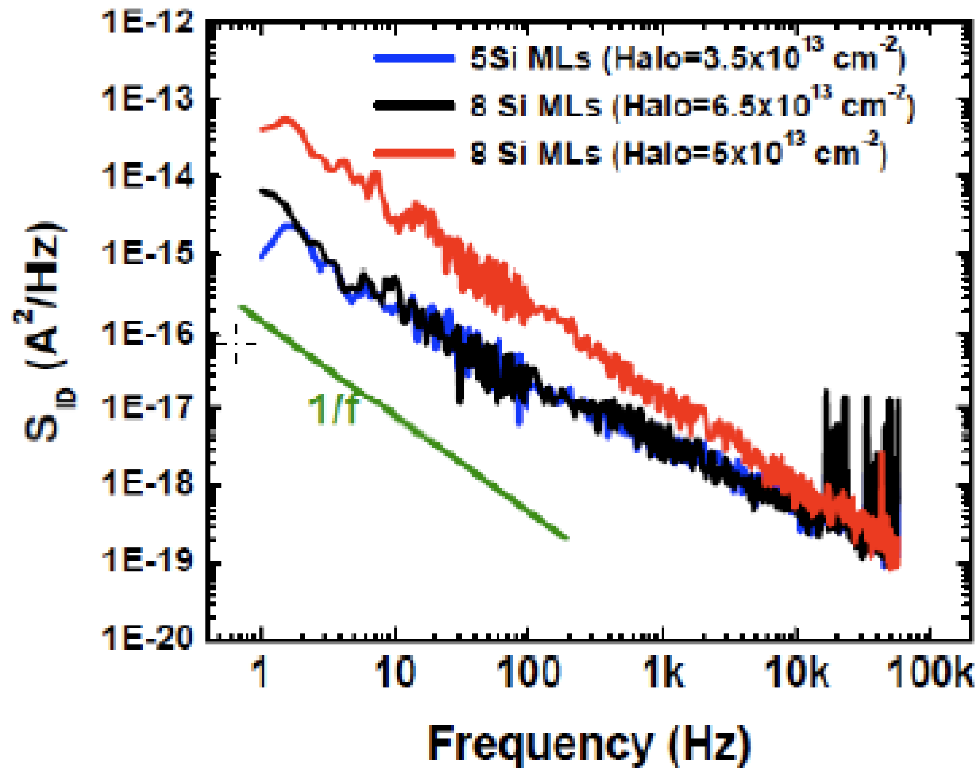
- 8 Si ML devices do not show significant mobility degradation
- Devices with 5 Si ML shows significant mobility degradation

Radiation Performance Ge Devices



Impact of the number of Si MLs and their deposition temperature on the pre-irradiation interface trap density.

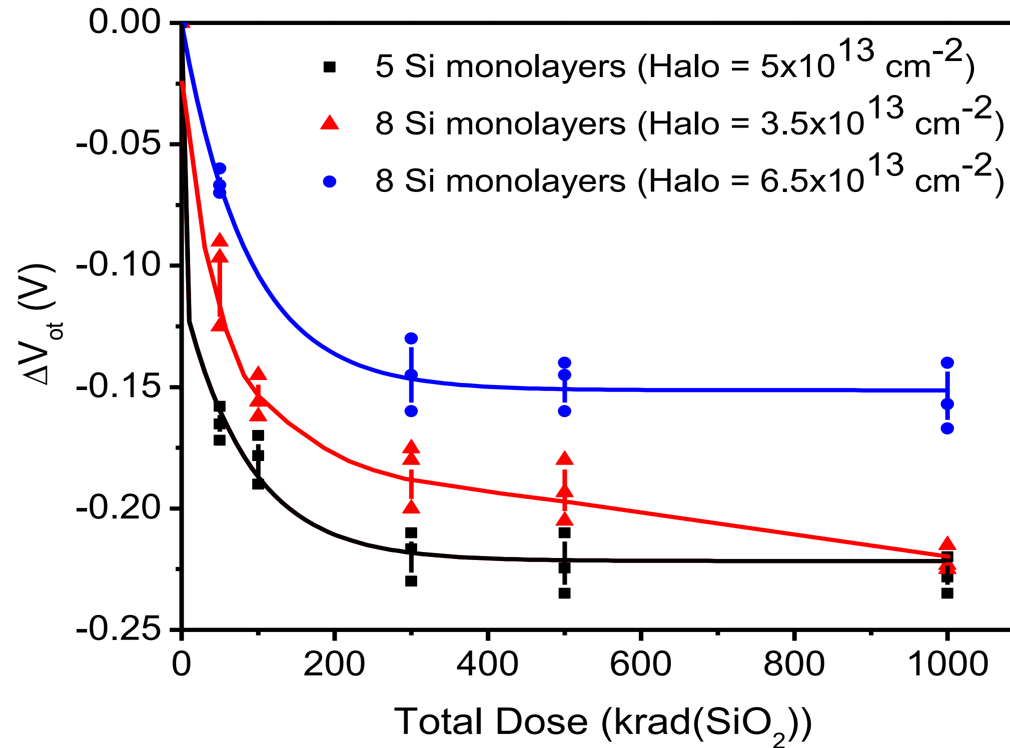
Pre-Radiation Performance Ge Devices – 1/f Noise



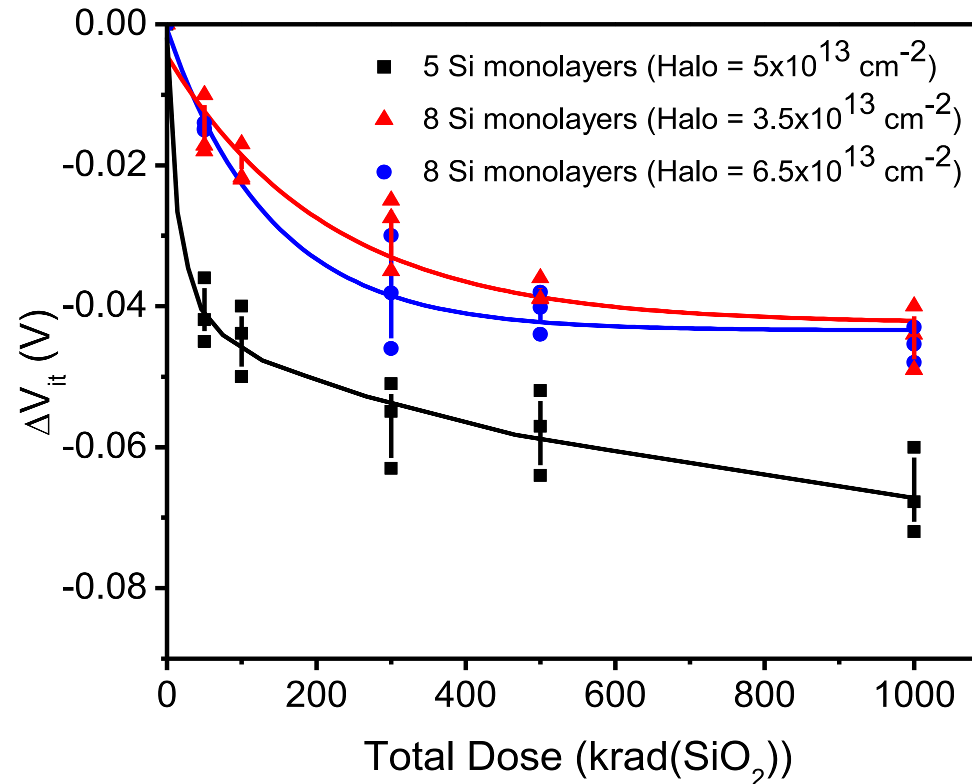
Pre-irradiation noise spectral density for the devices with different halo doping concentrations and thickness of Si capping layer.

C.X. Zhang, E.X. Zhang, D.M. Fleetwood, R.D. Schrimpf, K.F. Galloway, E. Simoen, J. Mitard and C. Claeys, IEEE Trans. Nucl. Sci., 57, 3066 (2010)

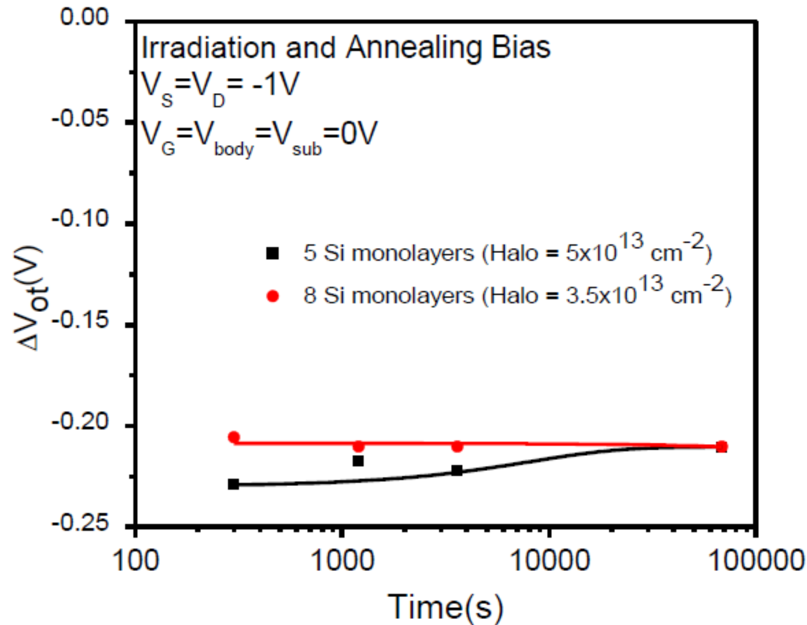
Radiation Performance Ge Devices – Oxide Traps

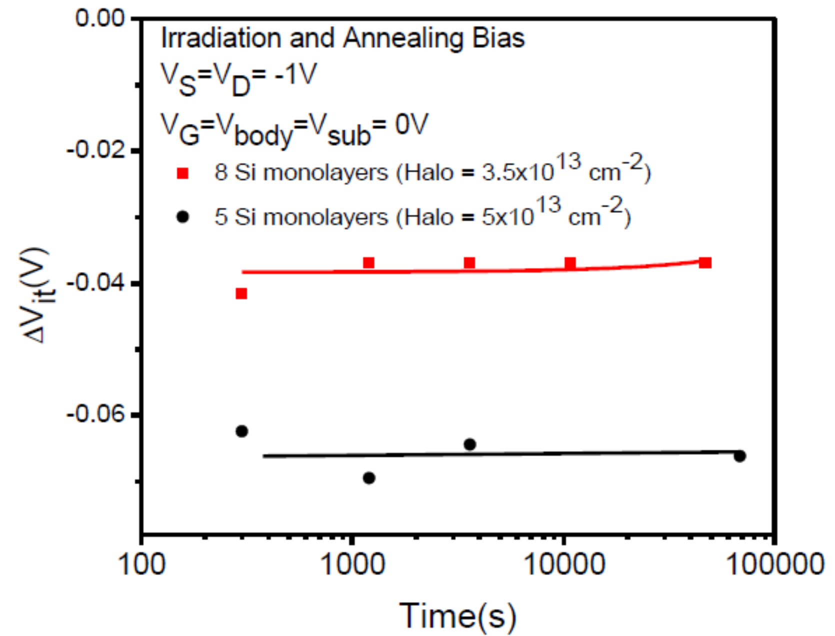


Radiation Performance Ge Devices – Interface Traps

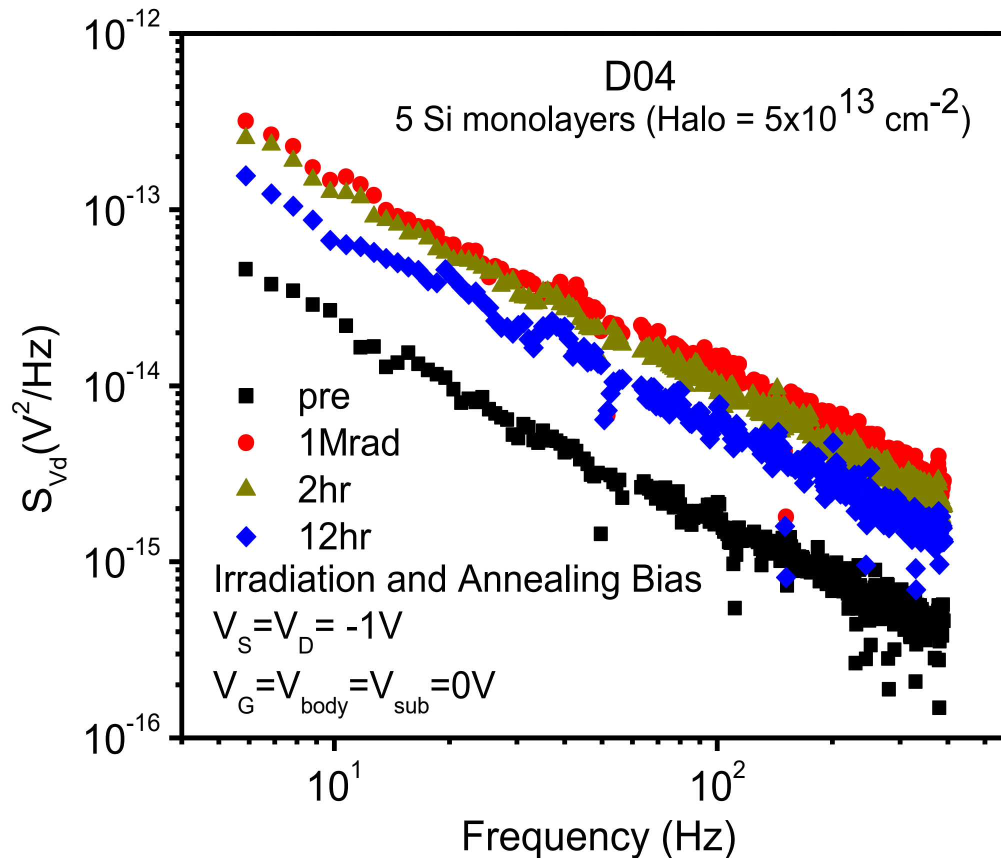


Annealing Performance Oxide and Interface Traps



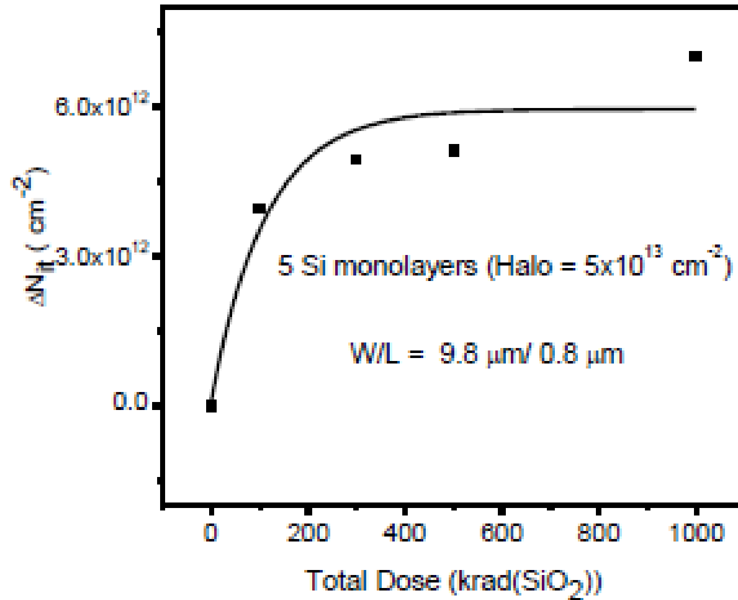


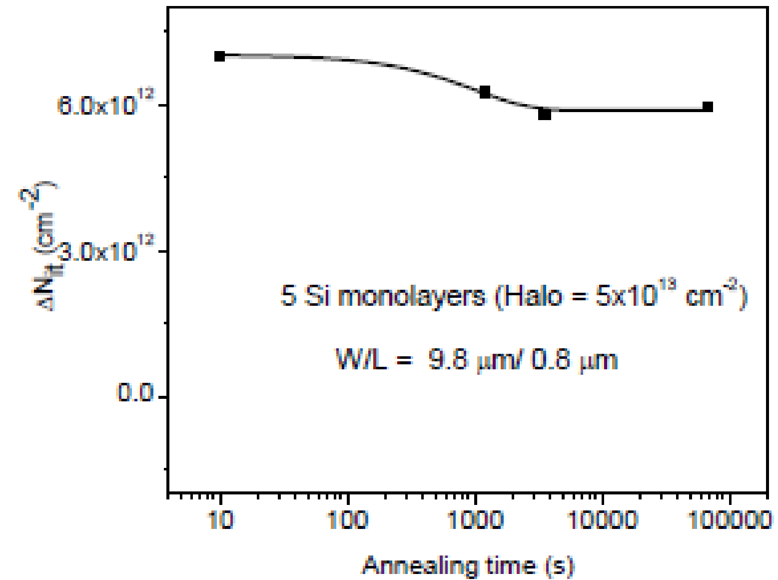
Radiation Performance Ge Devices – 1/f Noise



C.X. Zhang, E.X. Zhang, D.M. Fleetwood, R.D. Schrimpf, K.F. Galloway, E. Simoen, J. Mitard and C. Claeys, IEEE Trans. Nucl. Sci., 57, 3066 (2010)

Radiation Performance Ge Devices - ΔN_{it}

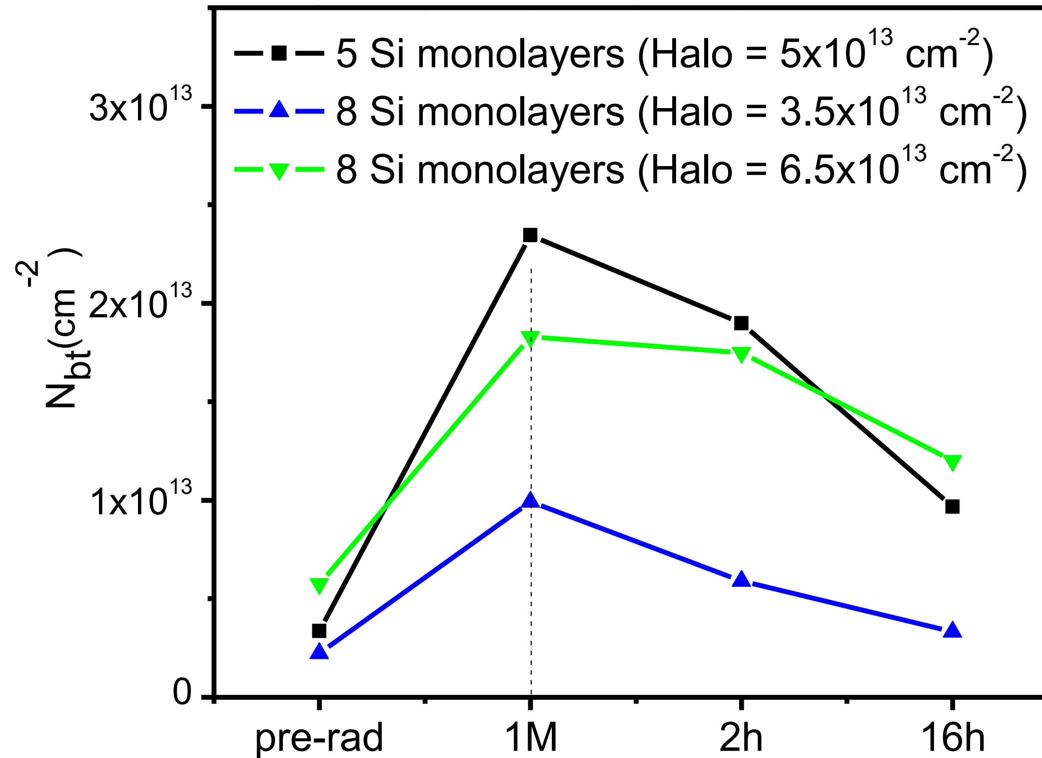




ΔN_{it} as a function of (a) total dose and (b) room-temperature annealing timefor a Ge pMOS device with W/L = 9.8 µm/0.8 µm.

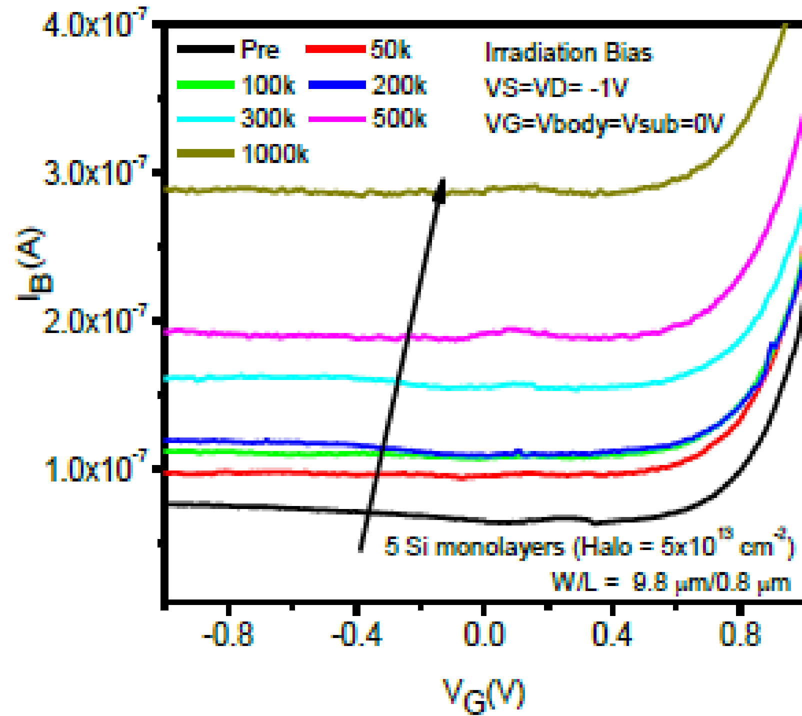
C.X. Zhang, E.X. Zhang, D.M. Fleetwood, R.D. Schrimpf, K.F. Galloway, E. Simoen, J. Mitard and C. Claeys, IEEE Trans. Nucl. Sci., 57, 3066 (2010)

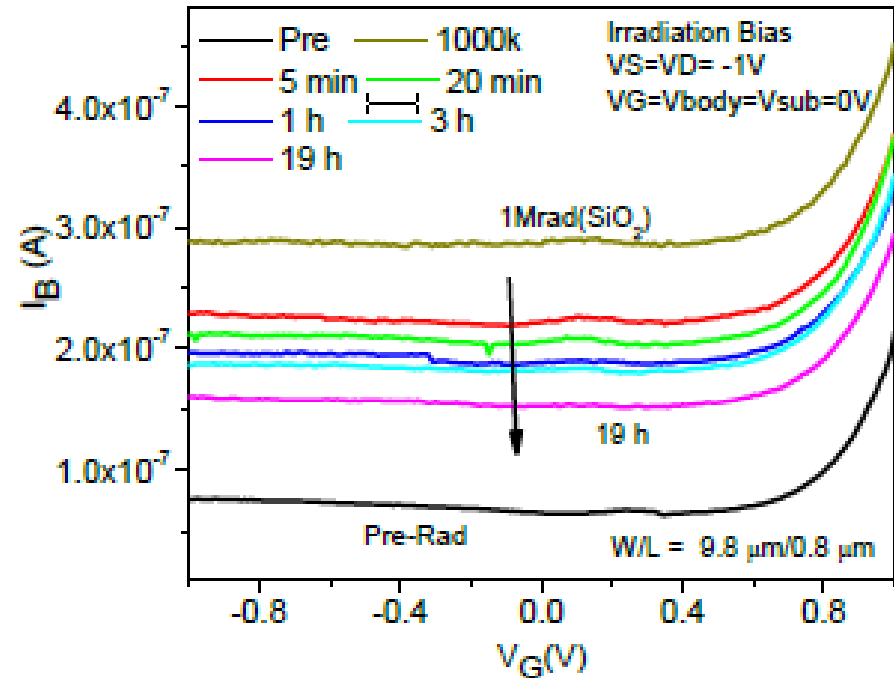
Radiation Performance Ge Devices – Bulk Traps



C.X. Zhang, E.X. Zhang, D.M. Fleetwood, R.D. Schrimpf, K.F. Galloway, E. Simoen, J. Mitard and C. Claeys, IEEE Trans. Nucl. Sci., 57, 3066 (2010)

X-Ray Radiation Ge Devices





Bulk current leakage I_B as a function of gate voltage V_G (a) as a function of irradiation and (b) as a function of isothermal annealing time at room temperature.

C.X. Zhang, E.X. Zhang, D.M. Fleetwood, R.D. Schrimpf, K.F. Galloway, E. Simoen, J. Mitard and C. Claeys, IEEE Trans. Nucl. Sci., 57, 3066 (2010)

Conclusions Ge Technology

- **The processing parameters (Si monolayers thickness and deposition temperature, halo conditions ...) have an impact on the radiation performance**

- **Radiation increases the interface trap density and the border traps**

- **Radiation-induced charge is Ge is higher than in Si devices, but still rather limited.**

- **Room temperature annealing has a positive impact**

General Conclusions

- Both the SiGe and the Ge technologies are sufficient radiation hard for space applications from a total dose point of view
- Radiation-induced variability is superimposed on the process-induced variability
- Radiation of 300 mm wafers enables to investigate a large number of devices and to increase the statistics
- Single Event Effects should also be investigated and may become dominant